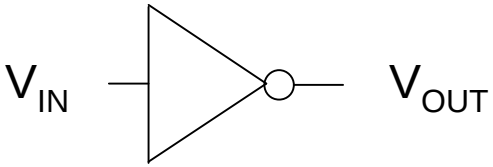
EE 434

Lecture 33

Logic Design

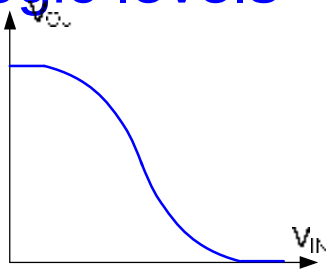
Review from last time:

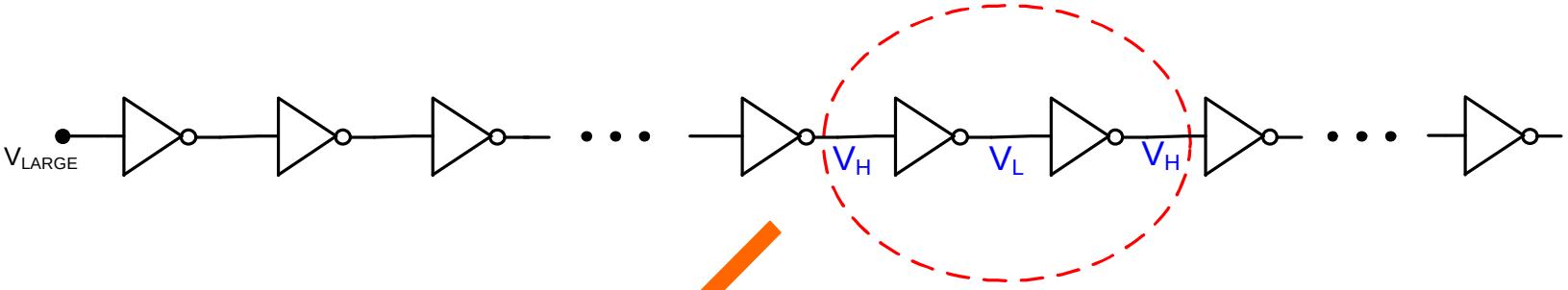
Ask the inverter how it will interpret logic levels

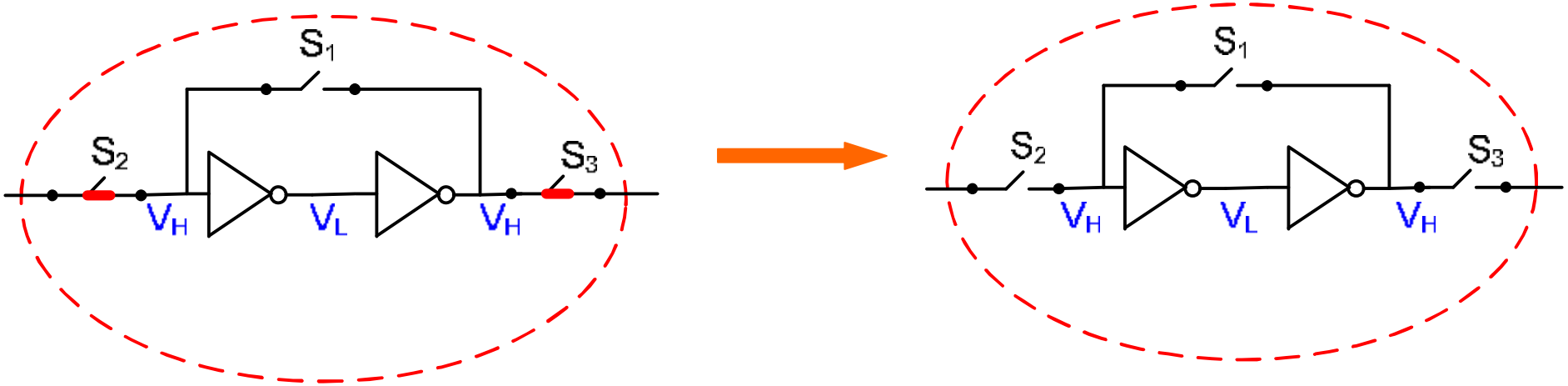


V_H=?

V_L=?

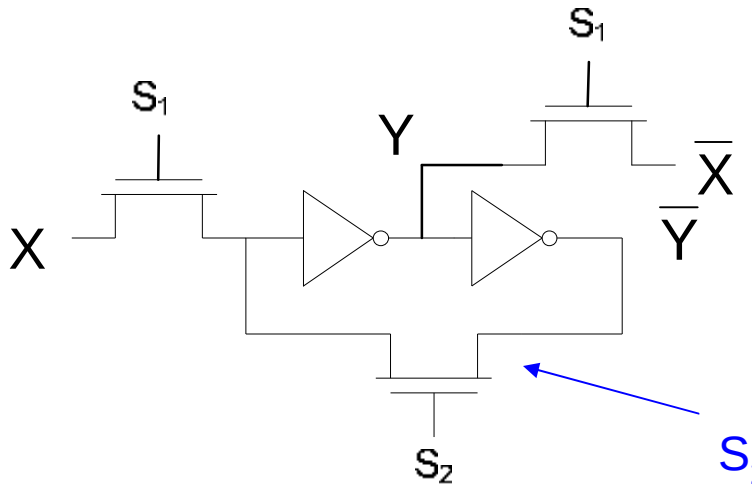




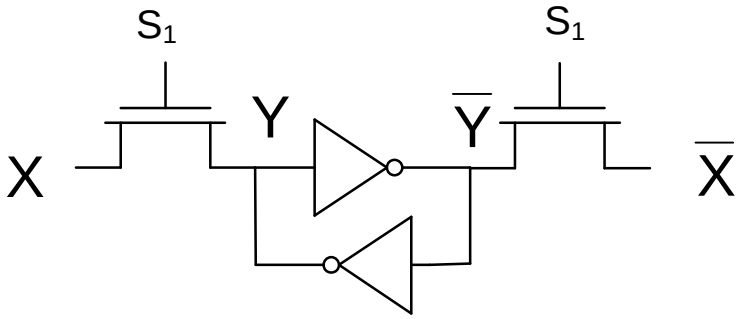


Review from last time:

The two-inverter loop



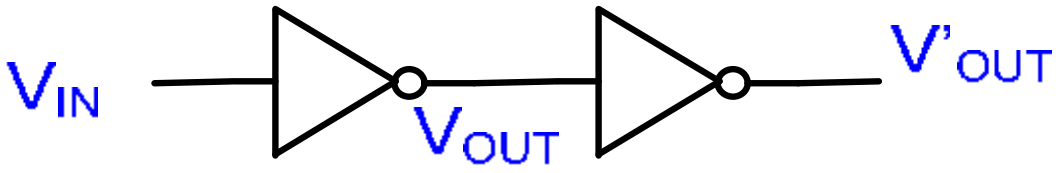
S_2 often eliminated (shorted)

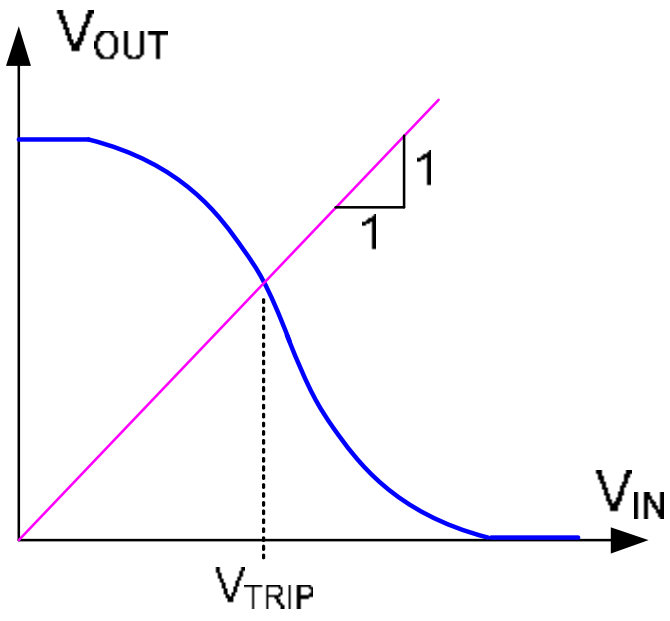


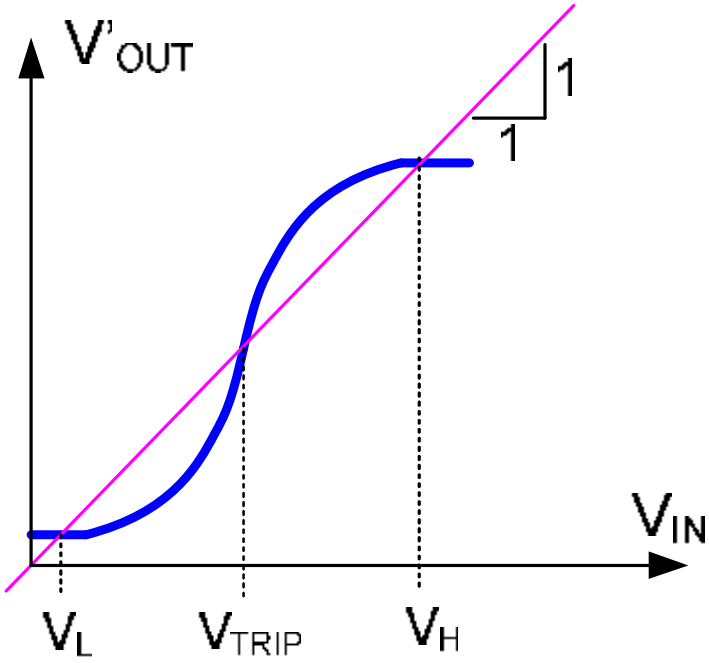
Standard 6-transistor SRAM Cell

Review from last time:

Observation







V_H and V_L obtained from the inverter pair transfer characteristics

V_{TRIP} can be obtained from either the inverter or the inverter pair transfer characteristics

Review from last time:

Logic Family Characteristics

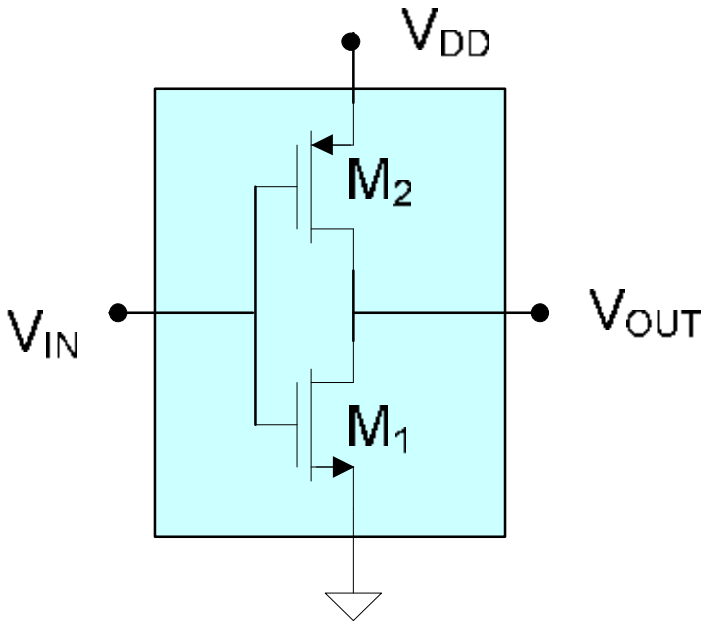
What properties of an inverter are necessary for it to be useful for building a two-level logic family

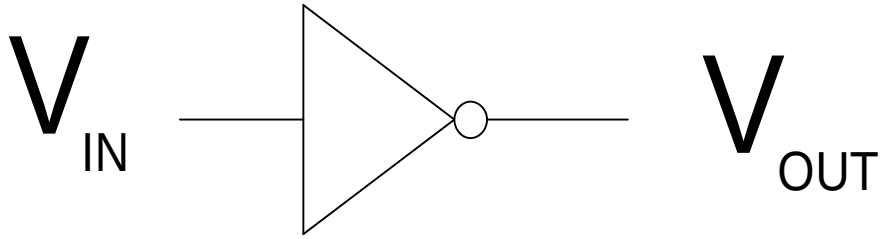
The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line

What are the logic levels for a given inverter of for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{OUT} = V_{IN}$ line

Transfer characteristics of the static CMOS inverter





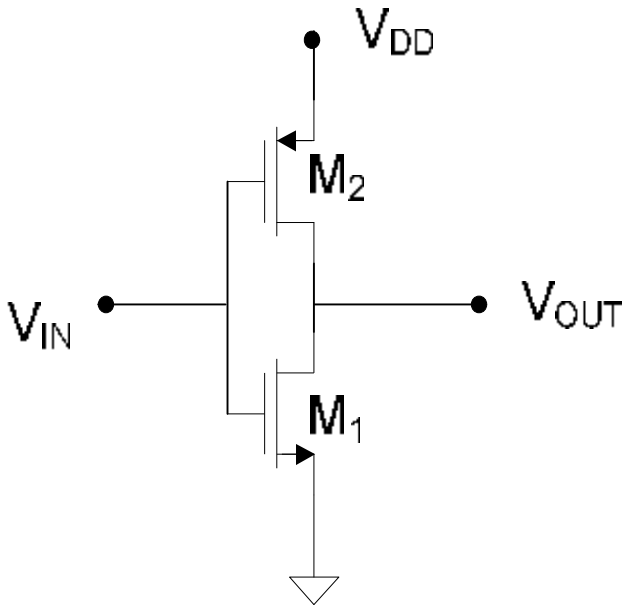
Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 1 M_1 triode, M_2 cutoff

$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = 0$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

It can be shown that the first solution will not verify, thus

$$V_{OUT} = 0$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \geq V_{Tp}$$

thus, valid for:

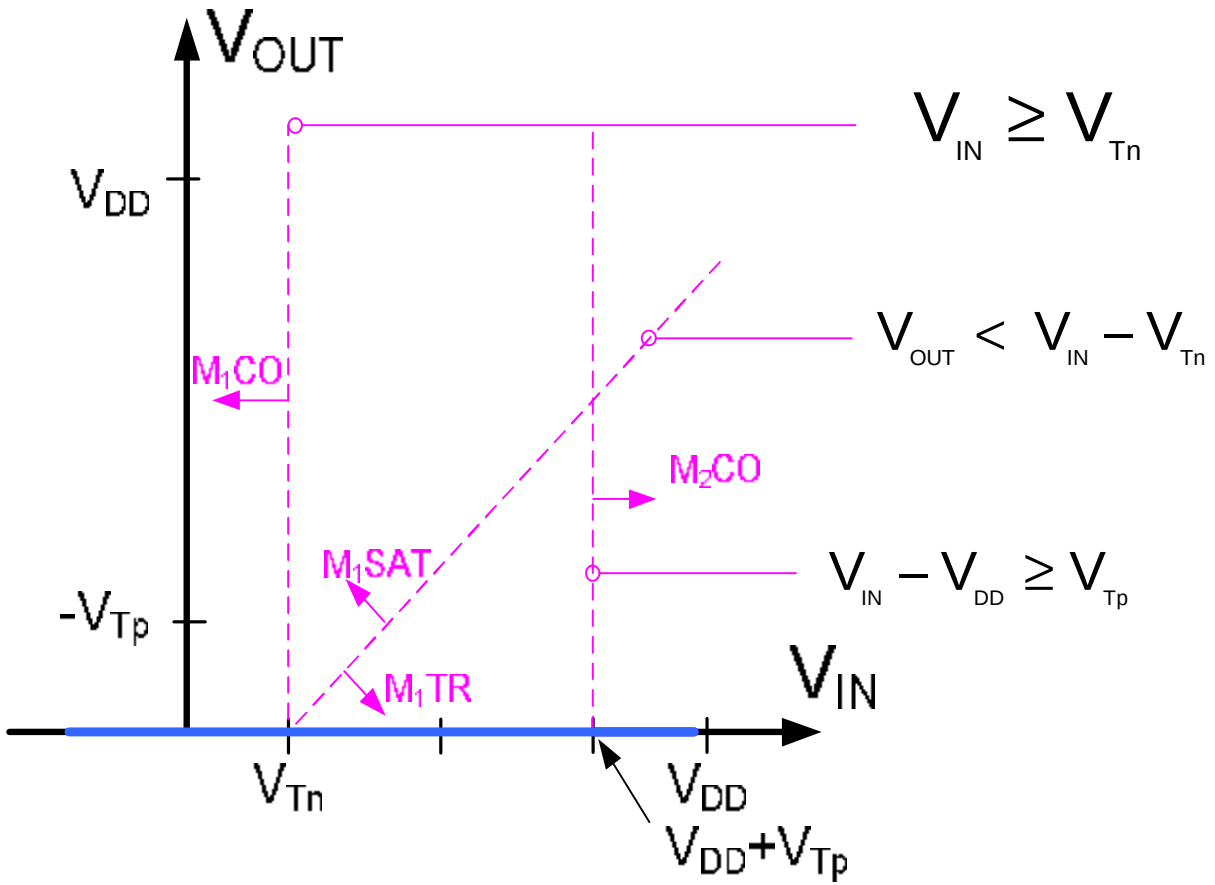
$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 1 M_1 triode, M_2 cutoff

$$V_{OUT} = 0$$

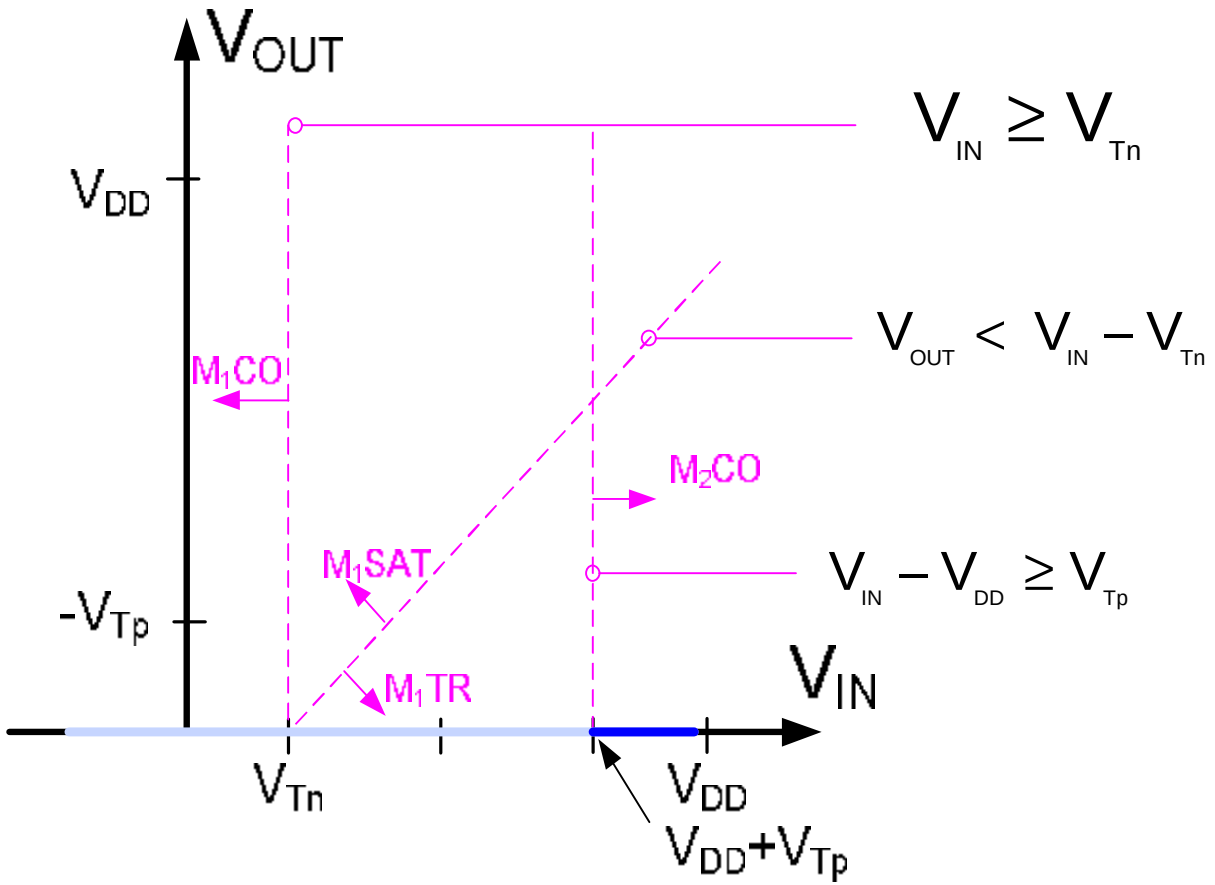


Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 1 M_1 triode, M_2 cutoff

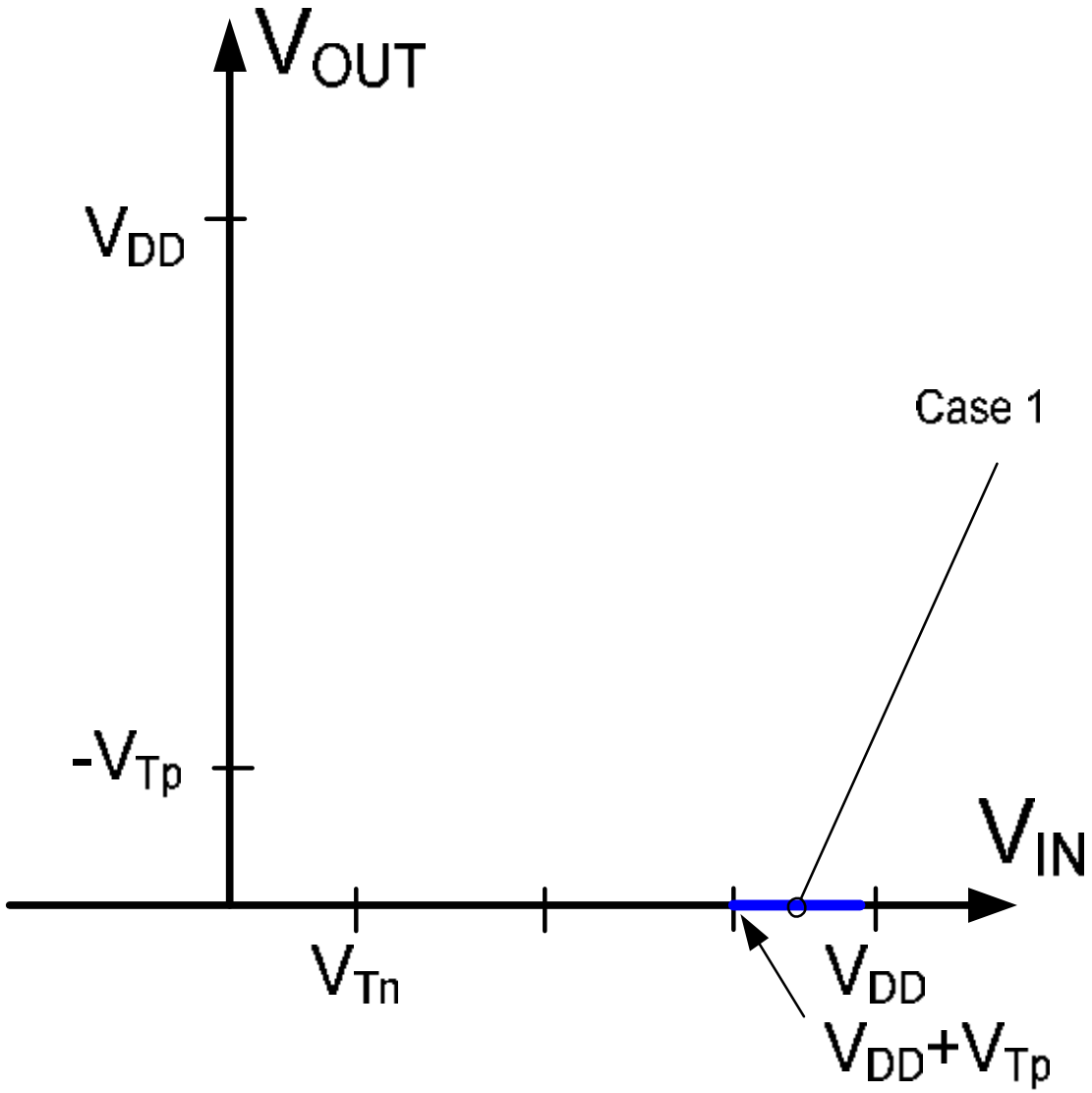
$$V_{OUT} = 0$$



Transfer characteristics of the static CMOS inverter

(Neglect effects)

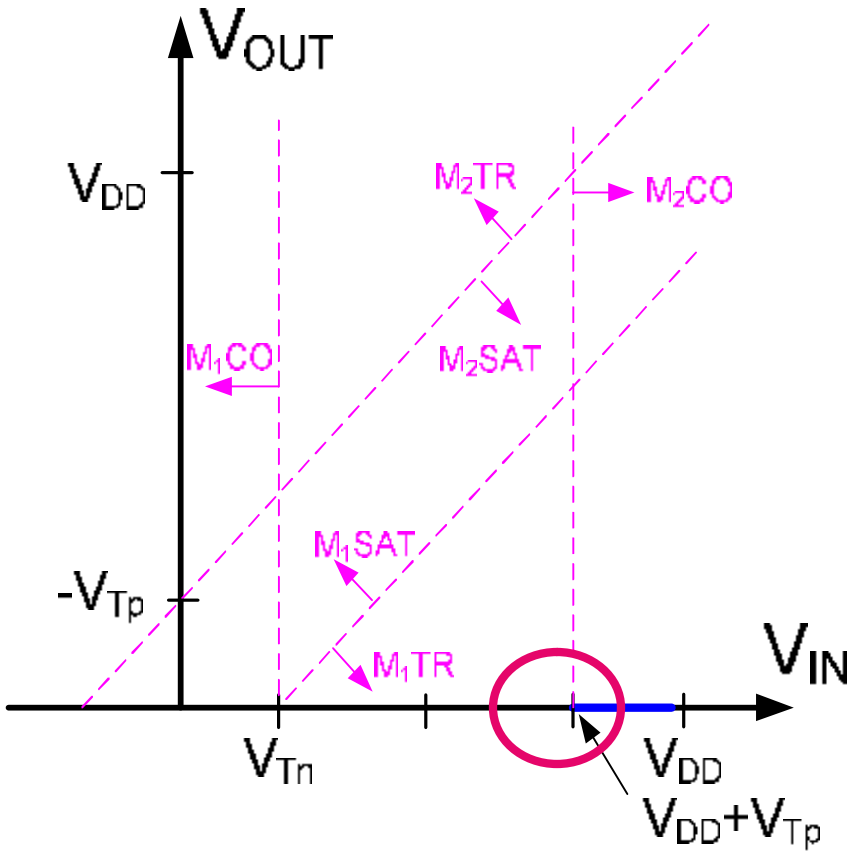
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect effects)

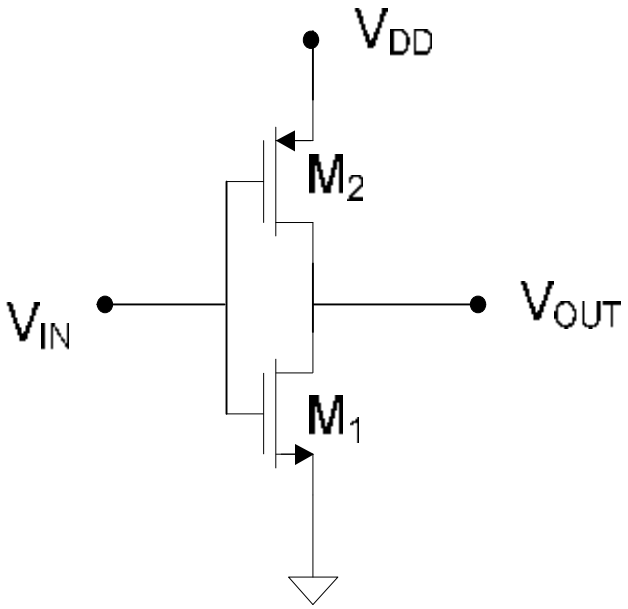
Case 2 M_1 triode, M_2 sat

$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} \left(V_{IN} - V_{DD} - V_{Tp} \right)^2$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} \left(V_{IN} - V_{DD} - V_{Tp} \right)^2 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$



valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} \leq V_{GS2} - V_{T2}$$

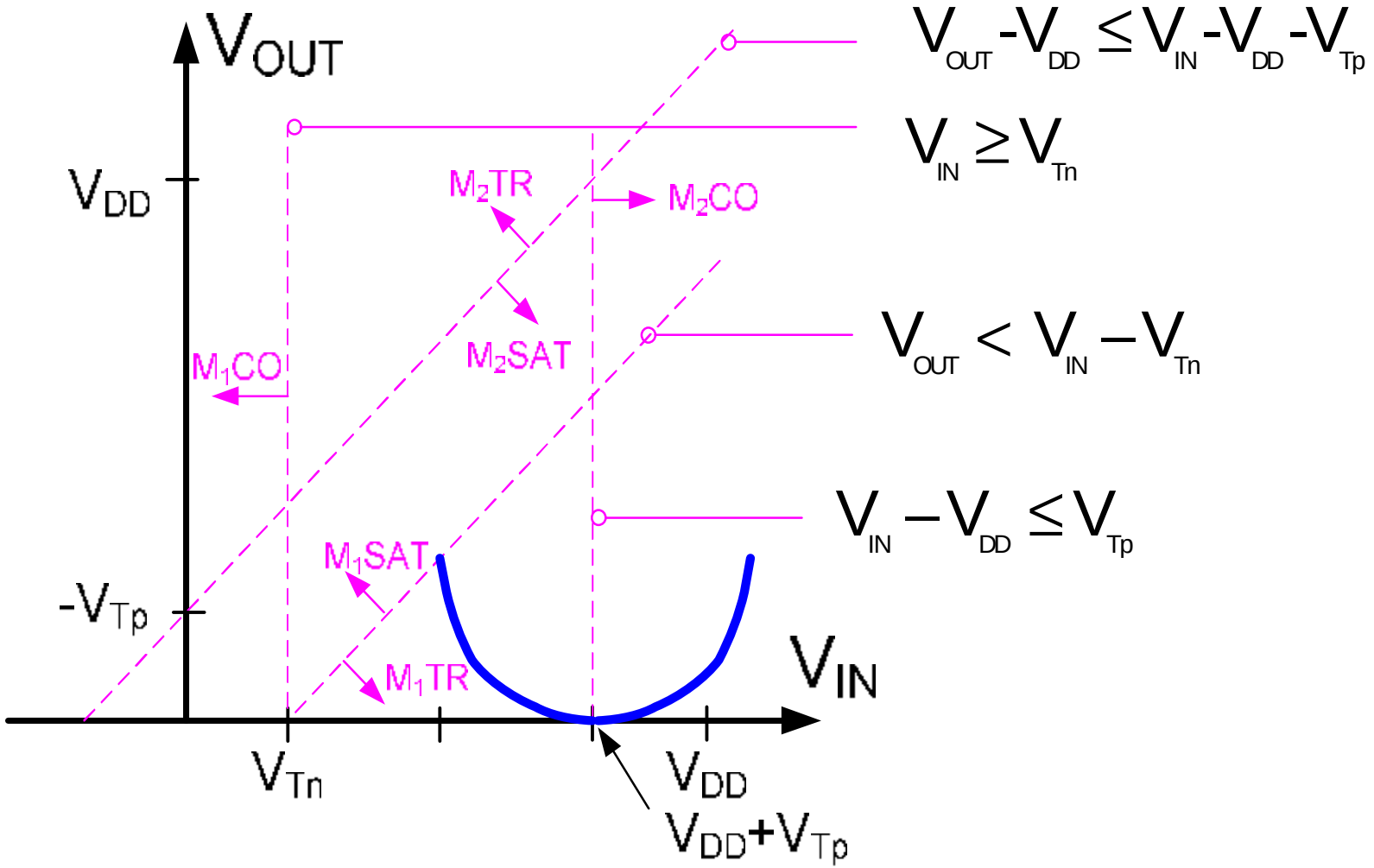
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect effects)

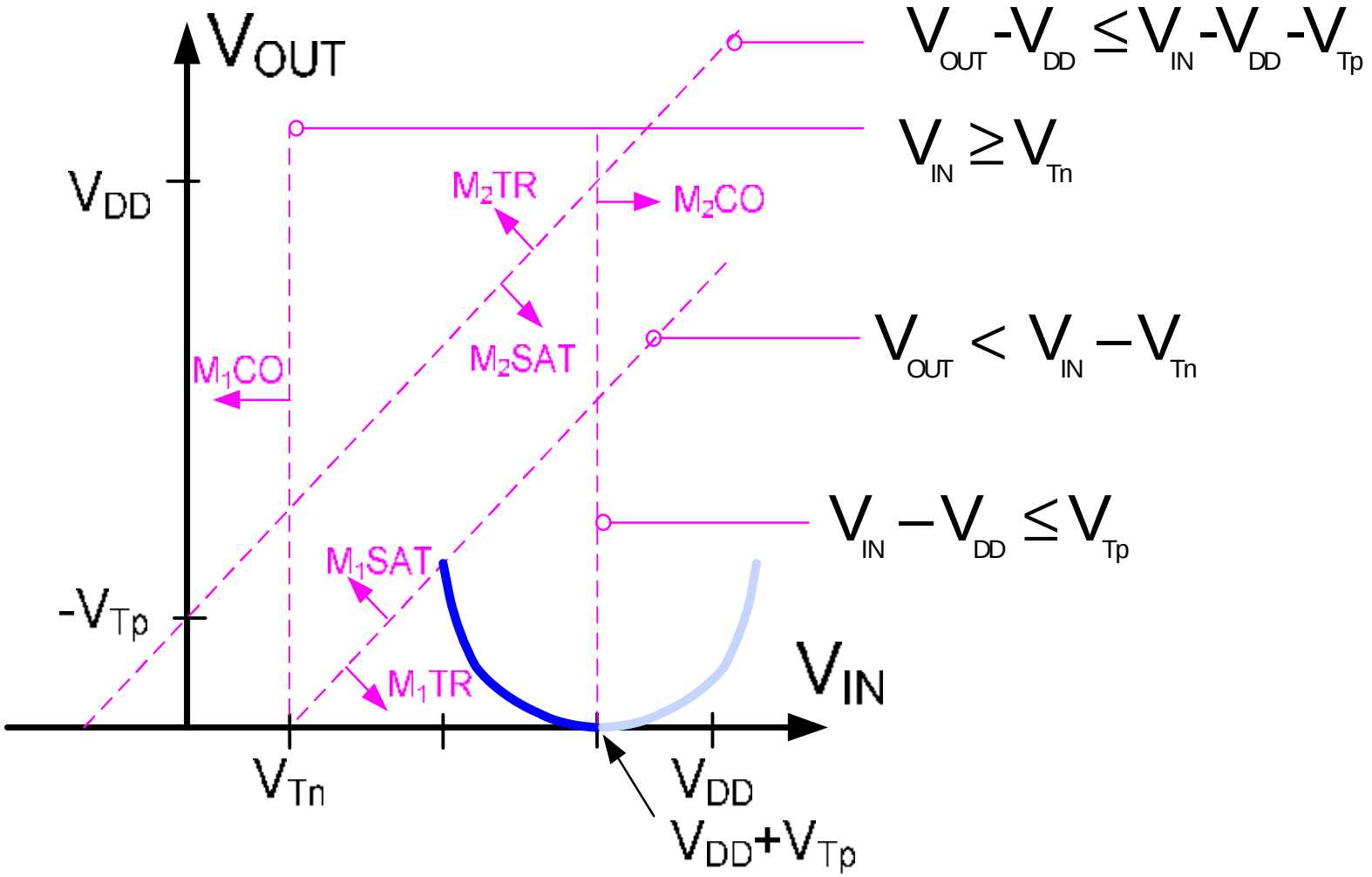
Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

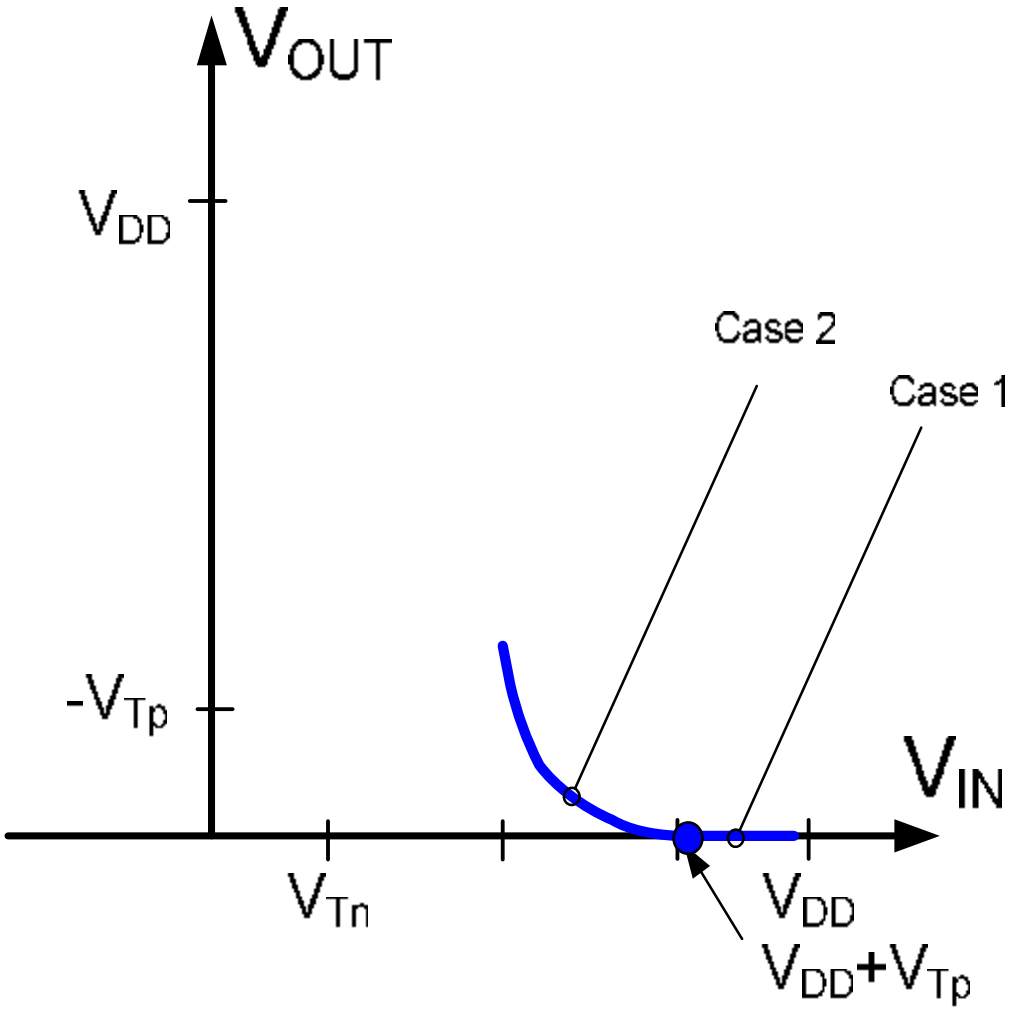
(Neglect effects)

Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

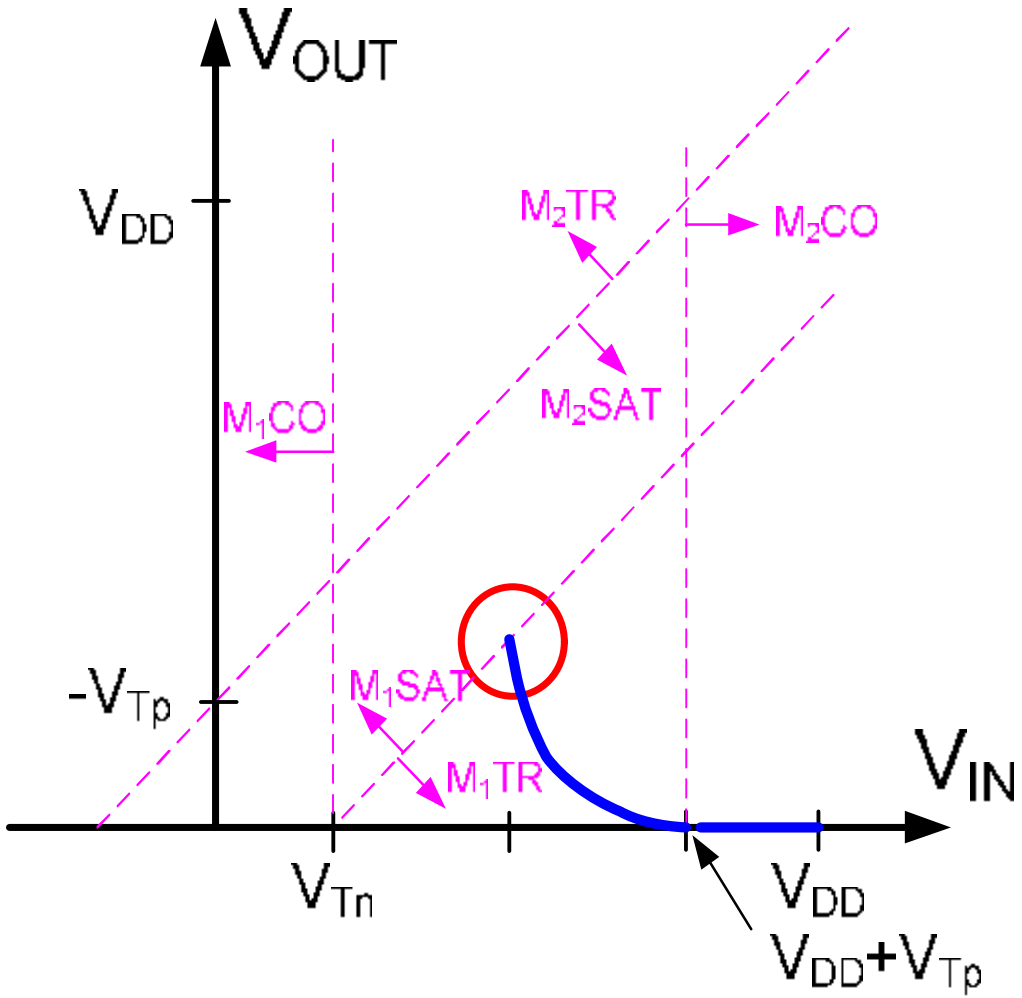
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 3 M_1 sat, M_2 sat

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = \frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2$$

Equating I_{D1} and $-I_{D2}$ we obtain:

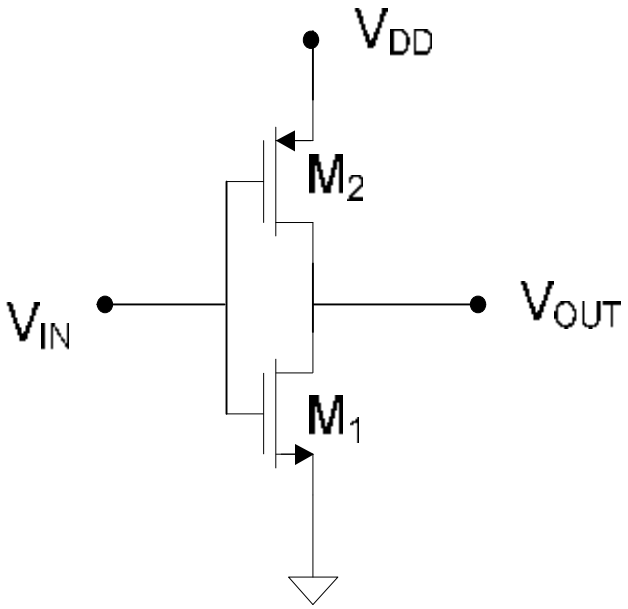
$$\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2 = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

Which can be rewritten as:

$$\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}\left(V_{DD} + V_{Tp} - V_{IN}\right) = \sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}}\left(V_{IN} - V_{Tn}\right)$$

Which can be simplified to:

$$V_{IN} = \frac{\left(V_{Tn}\right)\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$



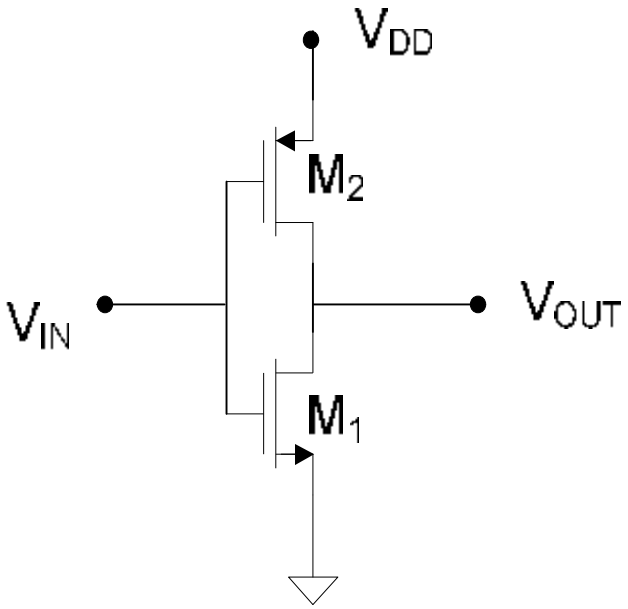
This is a vertical line

Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 3 M_1 sat, M_2 sat

$$V_{IN} = \frac{(V_{Tn})\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$



Since $C_{OXn} \cong C_{OXp} = C_{OX}$ this can be simplified to:

$$V_{IN} = \frac{(V_{Tn})\sqrt{\frac{W_1}{L_1}} + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}$$

valid for:

$V_{GS1} \geq V_{Tn}$ $V_{DS1} \geq V_{GS1} - V_{Tn}$ $V_{GS2} \leq V_{Tp}$ $V_{DS2} \leq V_{GS2} - V_{T2}$

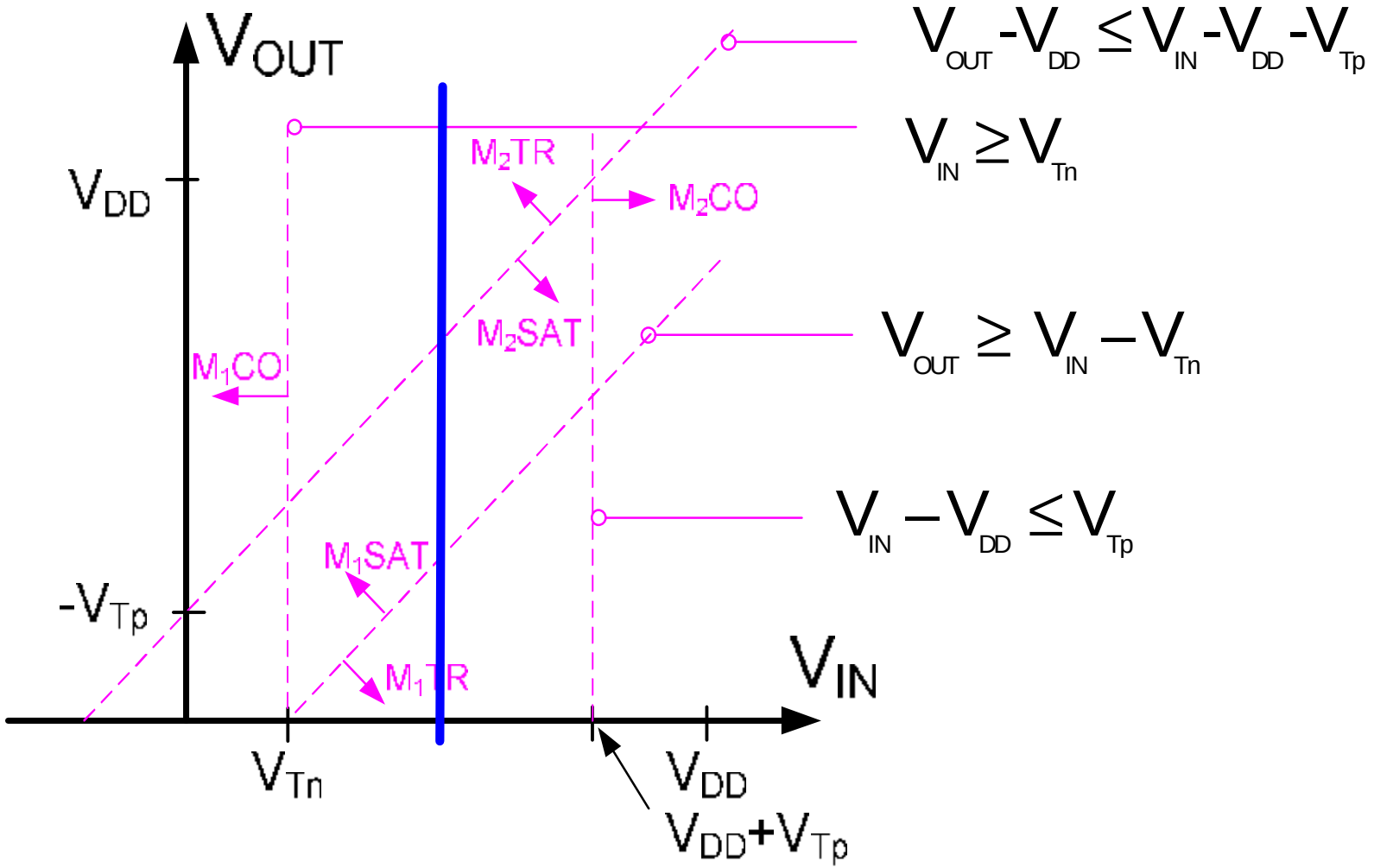
thus, valid for:

$V_{IN} \geq V_{Tn}$ $V_{OUT} \geq V_{IN} - V_{Tn}$ $V_{IN} - V_{DD} \leq V_{Tp}$ $V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$

Transfer characteristics of the static CMOS inverter

(Neglect effects)

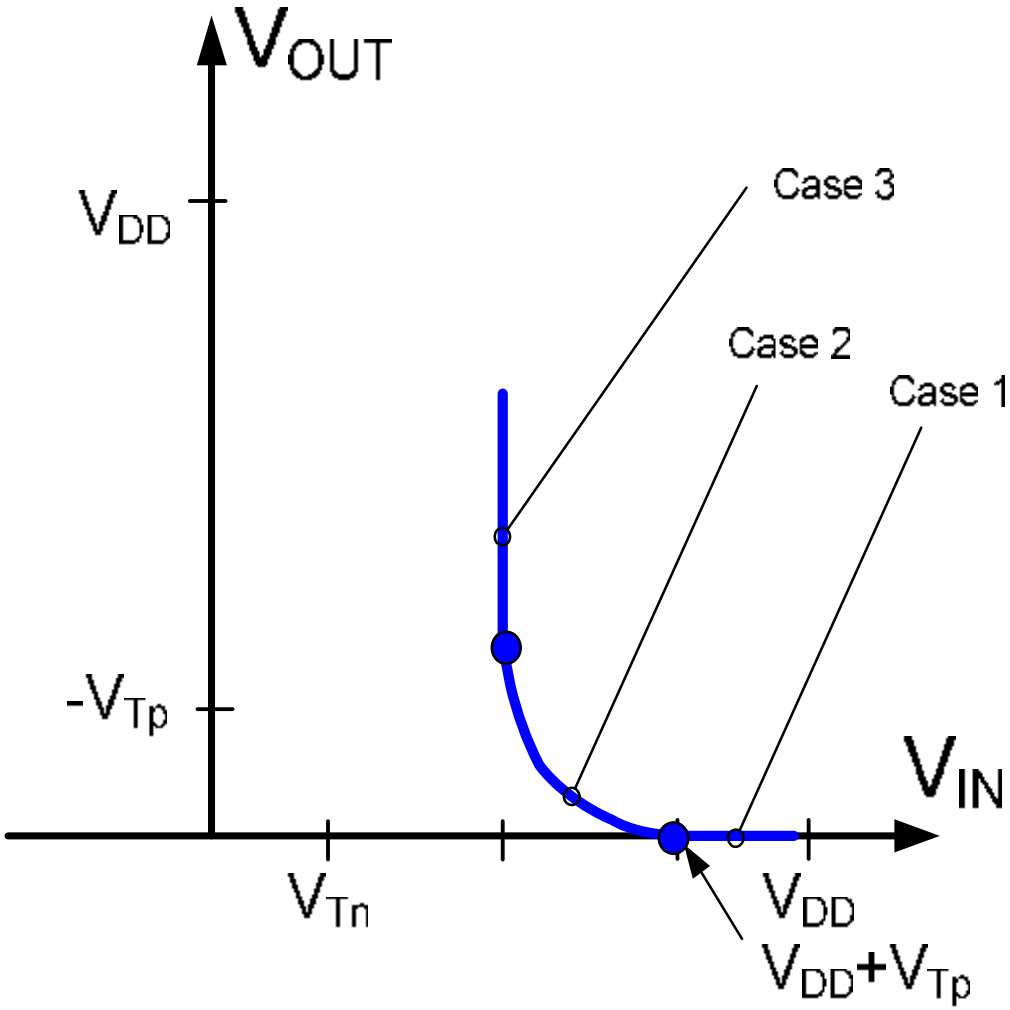
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect effects)

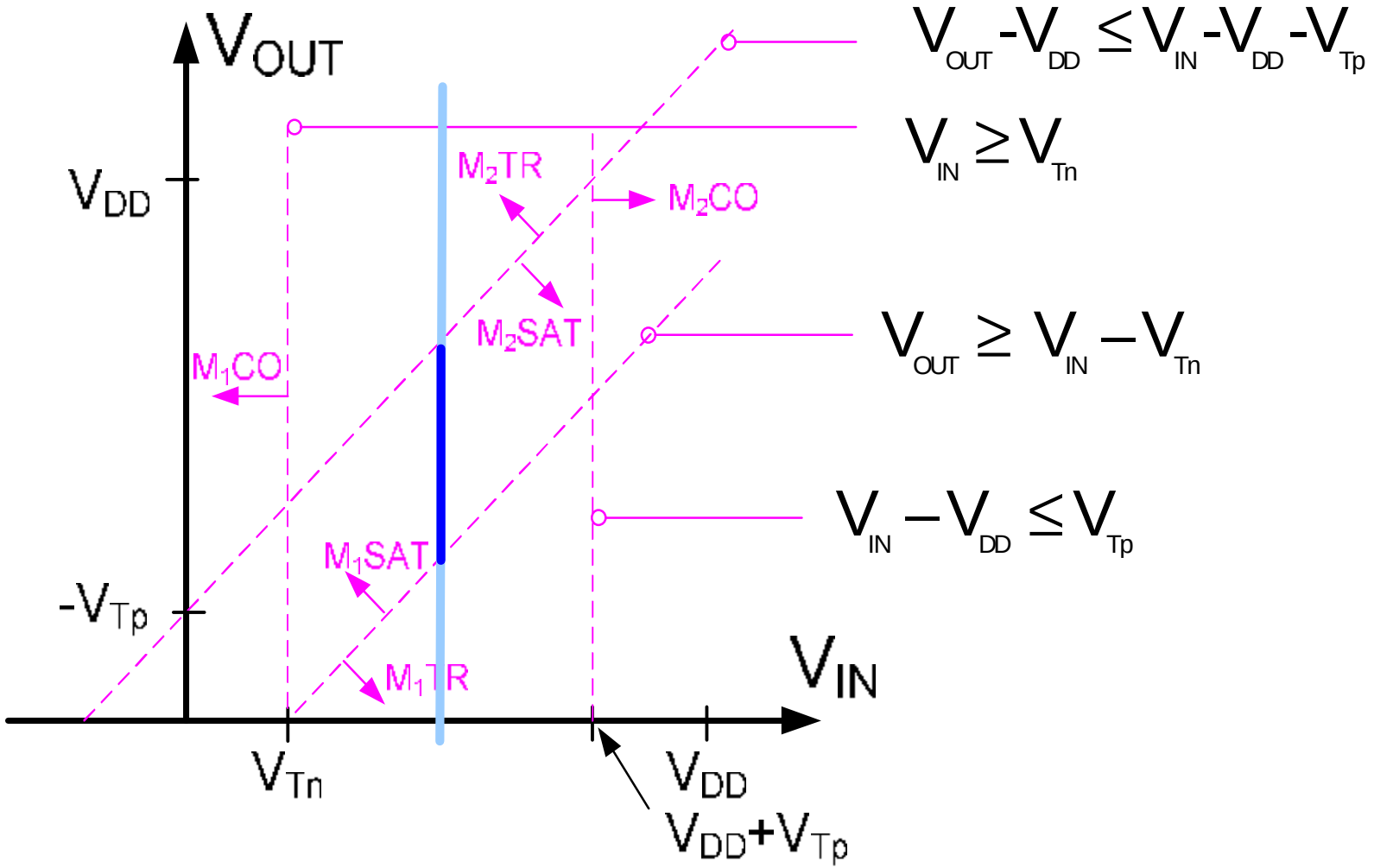
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect effects)

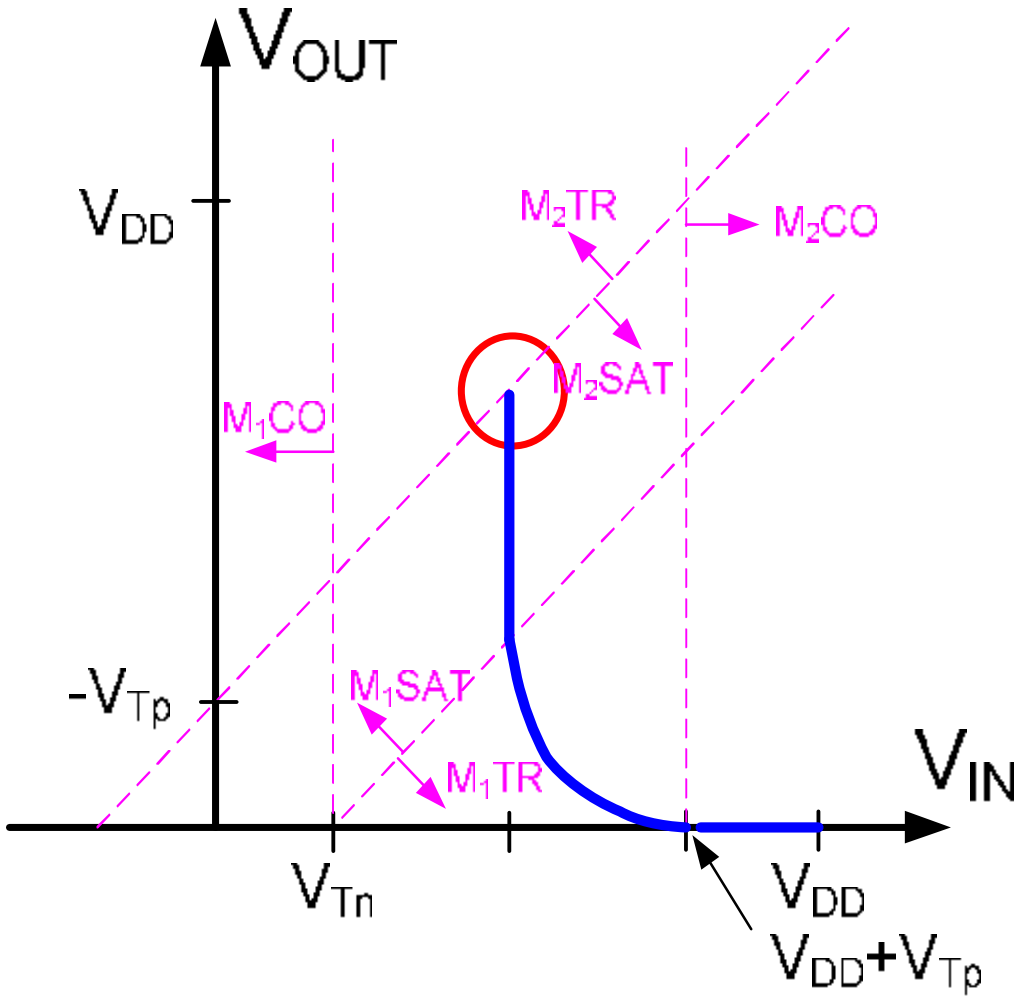
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 4 M_1 sat, M_2 triode



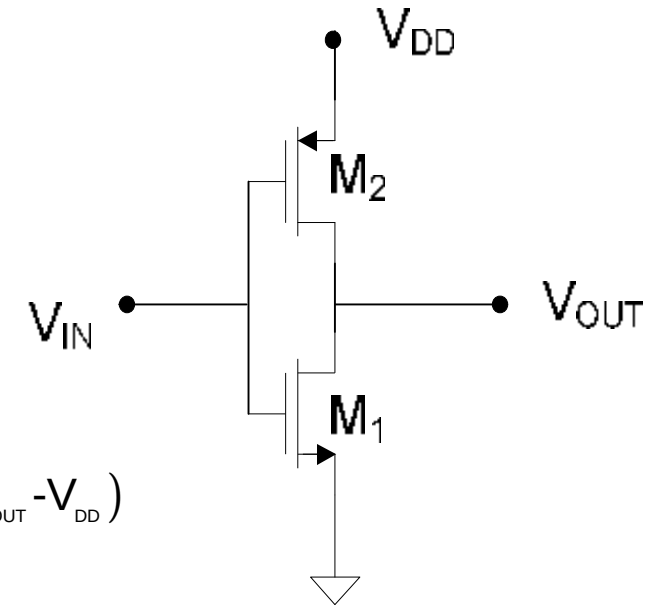
Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 4 M_1 sat, M_2 triode

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = -\mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2 = \mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} \geq V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} > V_{GS2}\text{-}V_{T2}$$

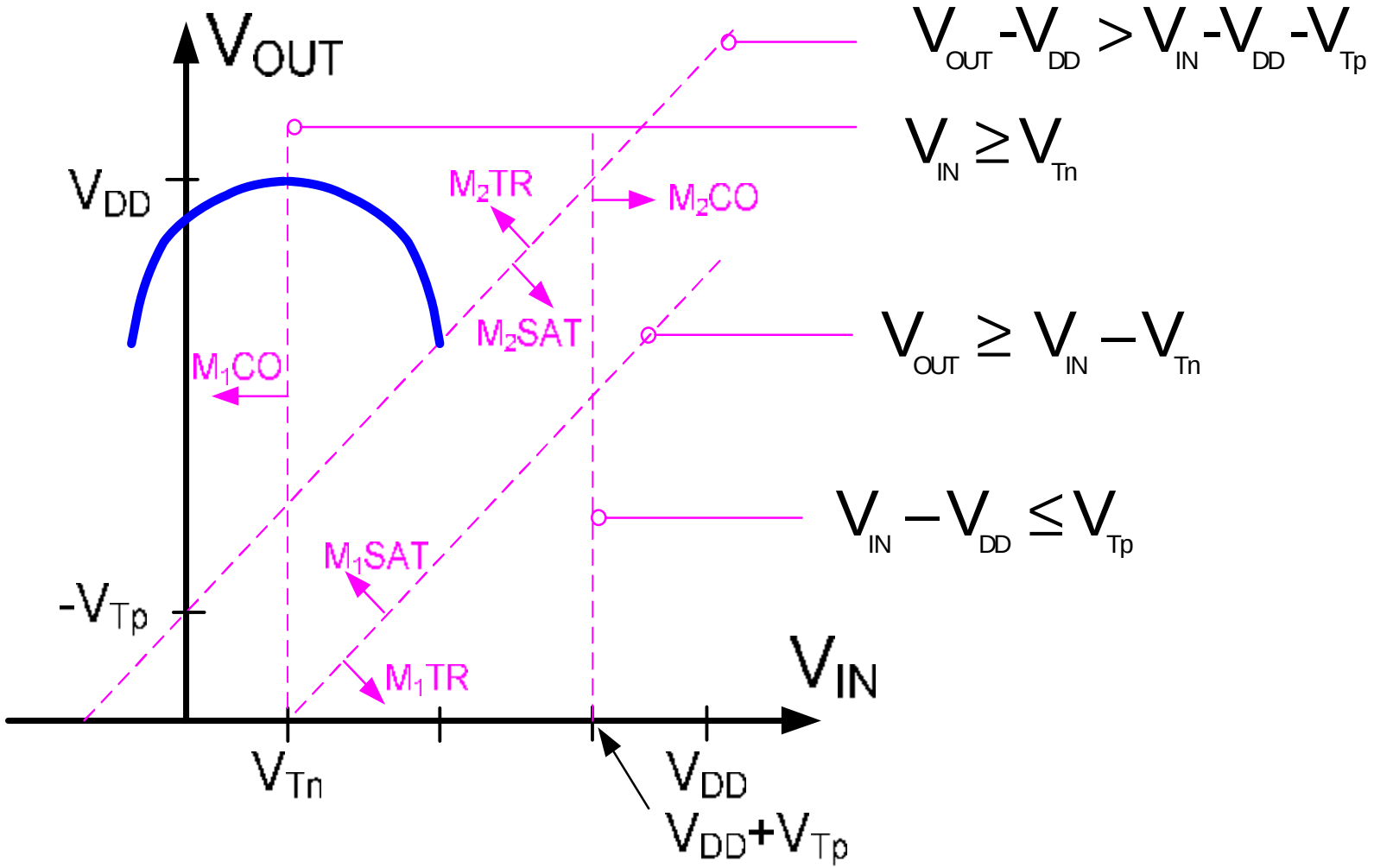
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} \geq V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT}\text{-}V_{DD} > V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect effects)

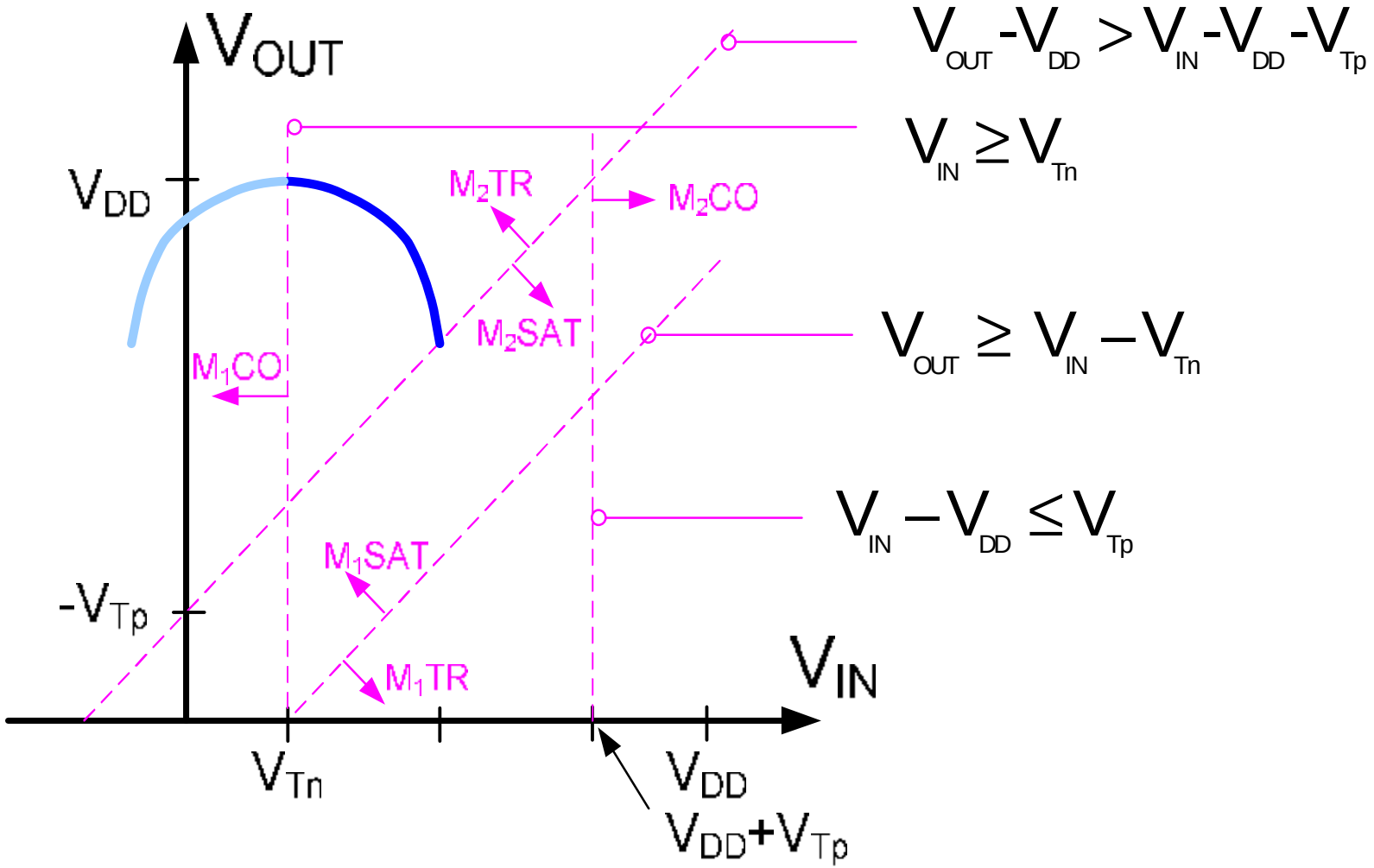
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect effects)

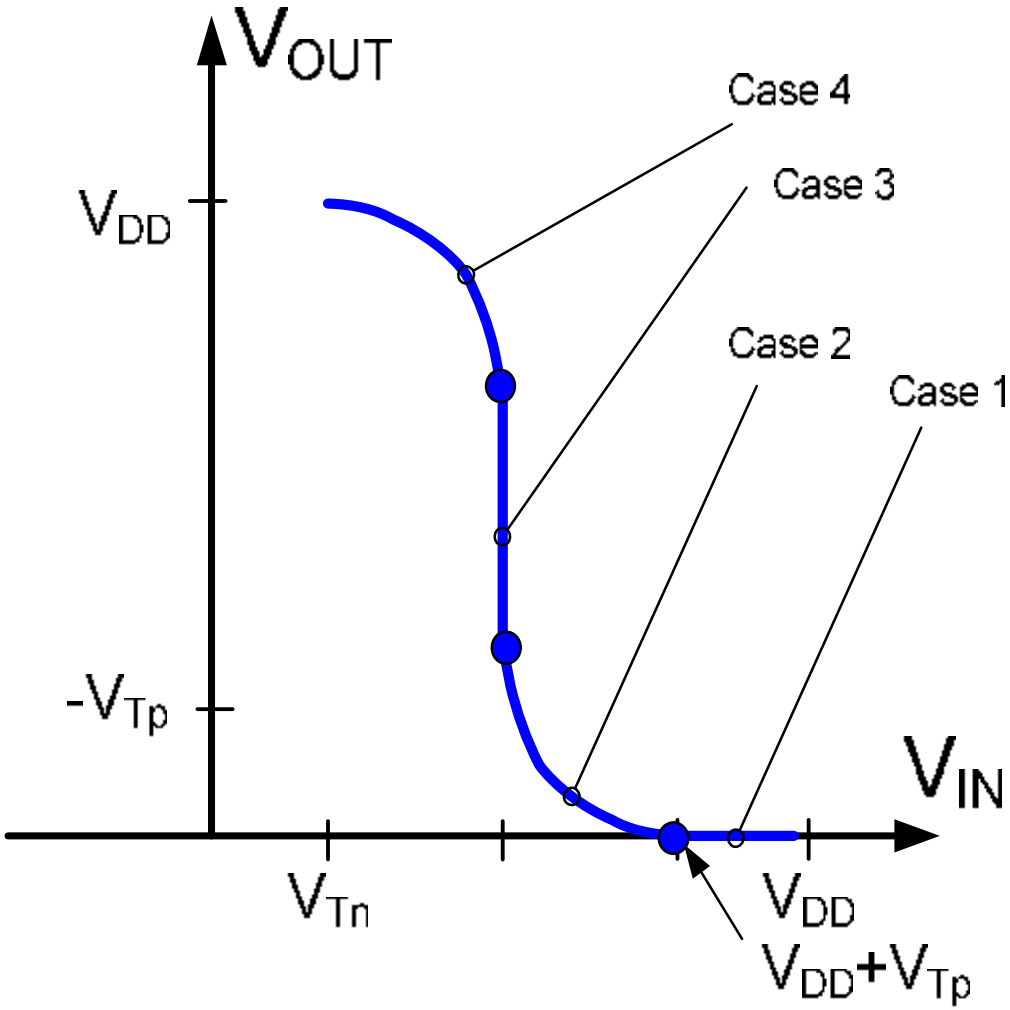
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect effects)

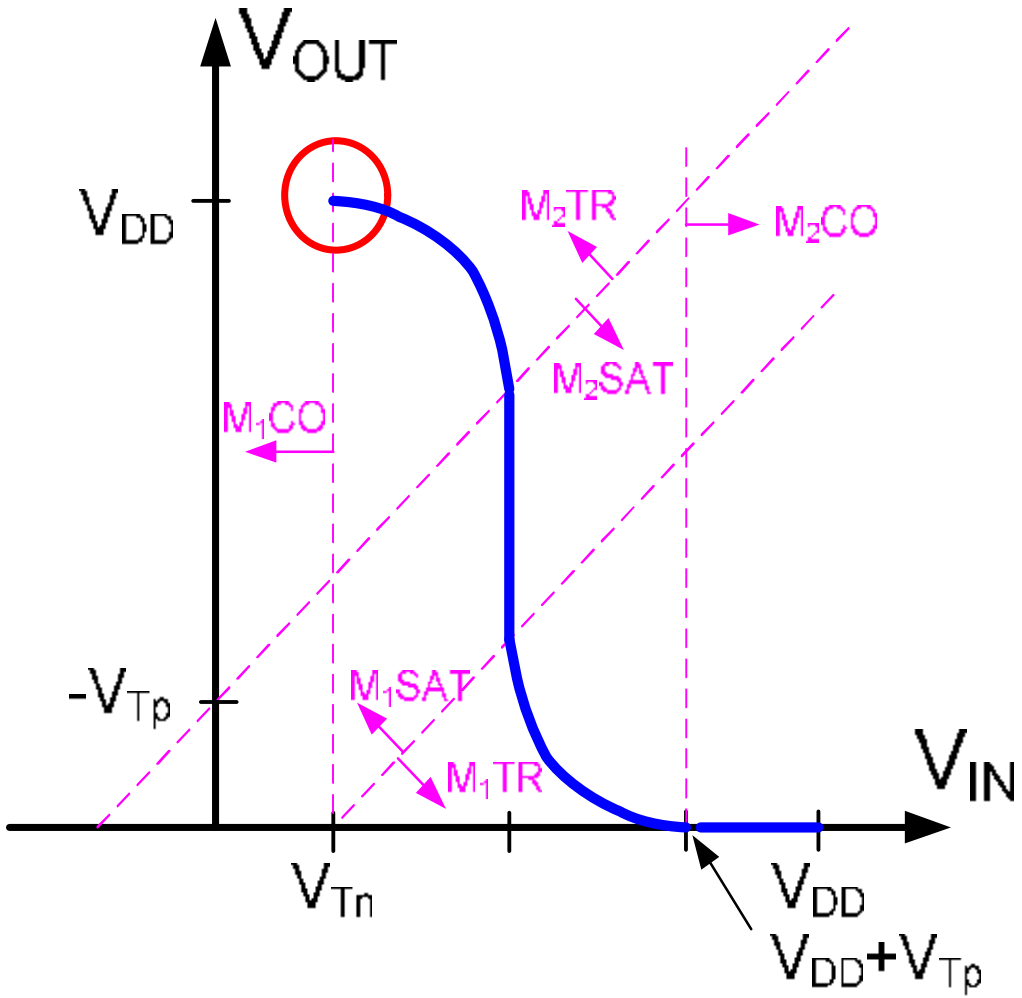
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect effects)

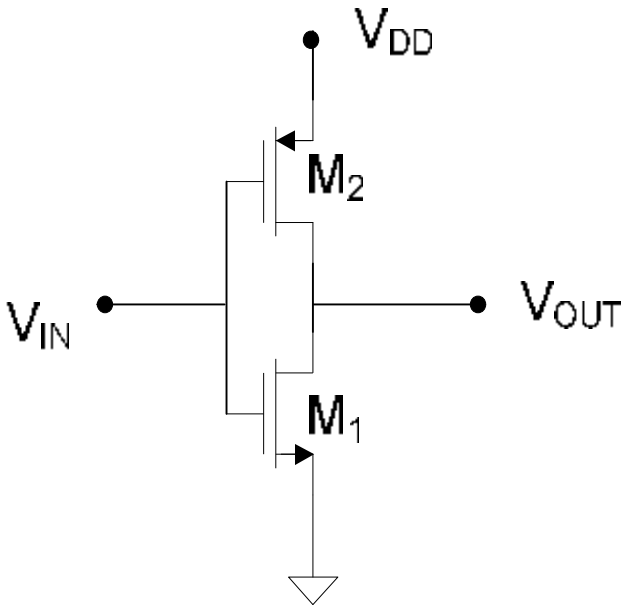
Case 4 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect effects)

Case 5 M_1 cutoff, M_2 triode



$$I_{D1} = 0$$

$$I_{D2} = -\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2} \right) \bullet \left(V_{OUT}\text{-}V_{DD} \right)$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2} \right) \bullet \left(V_{OUT}\text{-}V_{DD} \right) = 0$$

valid for:

$$V_{GS1} < V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} > V_{GS2}\text{-}V_{T2}$$

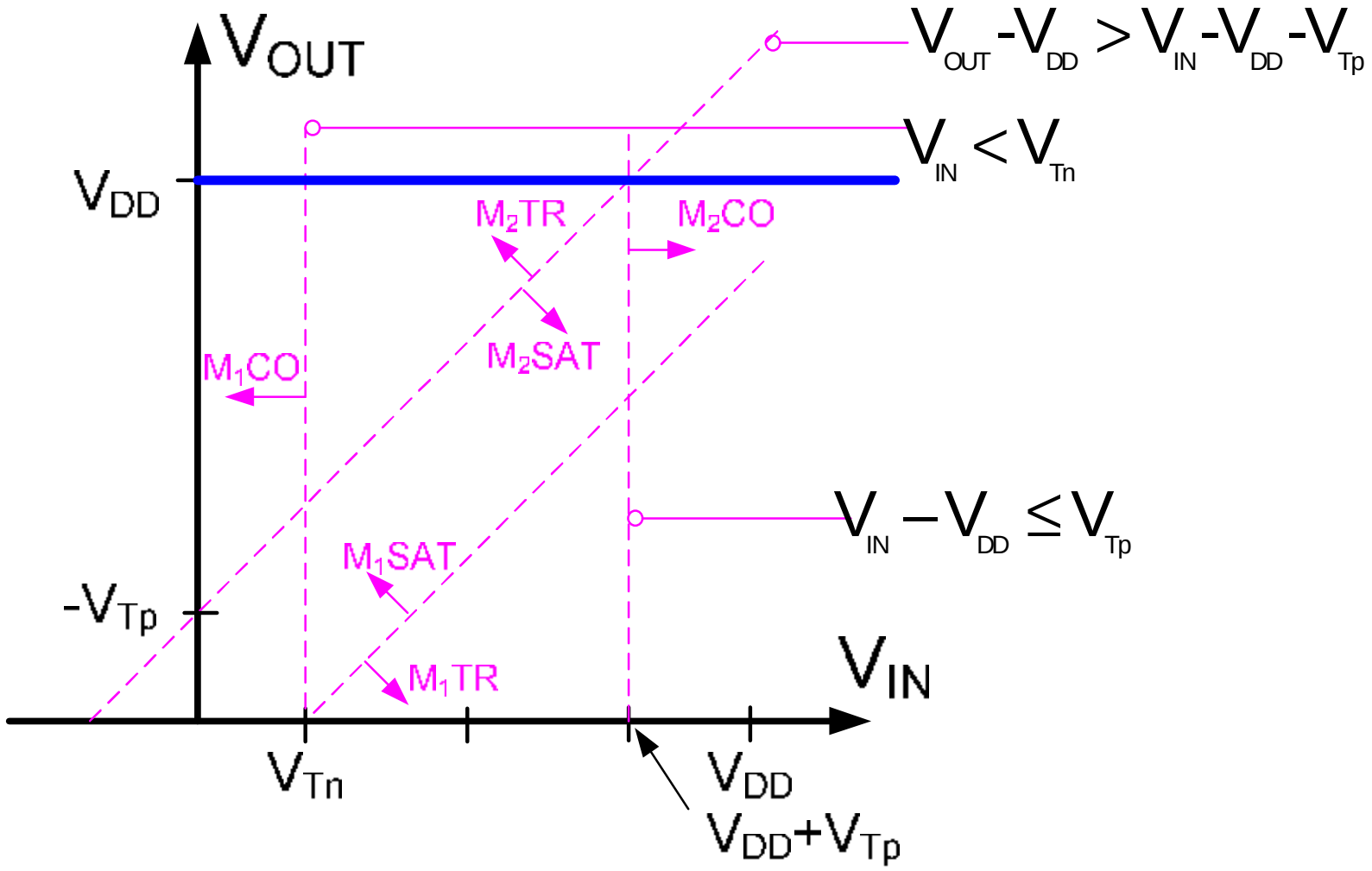
thus, valid for:

$$V_{IN} < V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT}\text{-}V_{DD} > V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect effects)

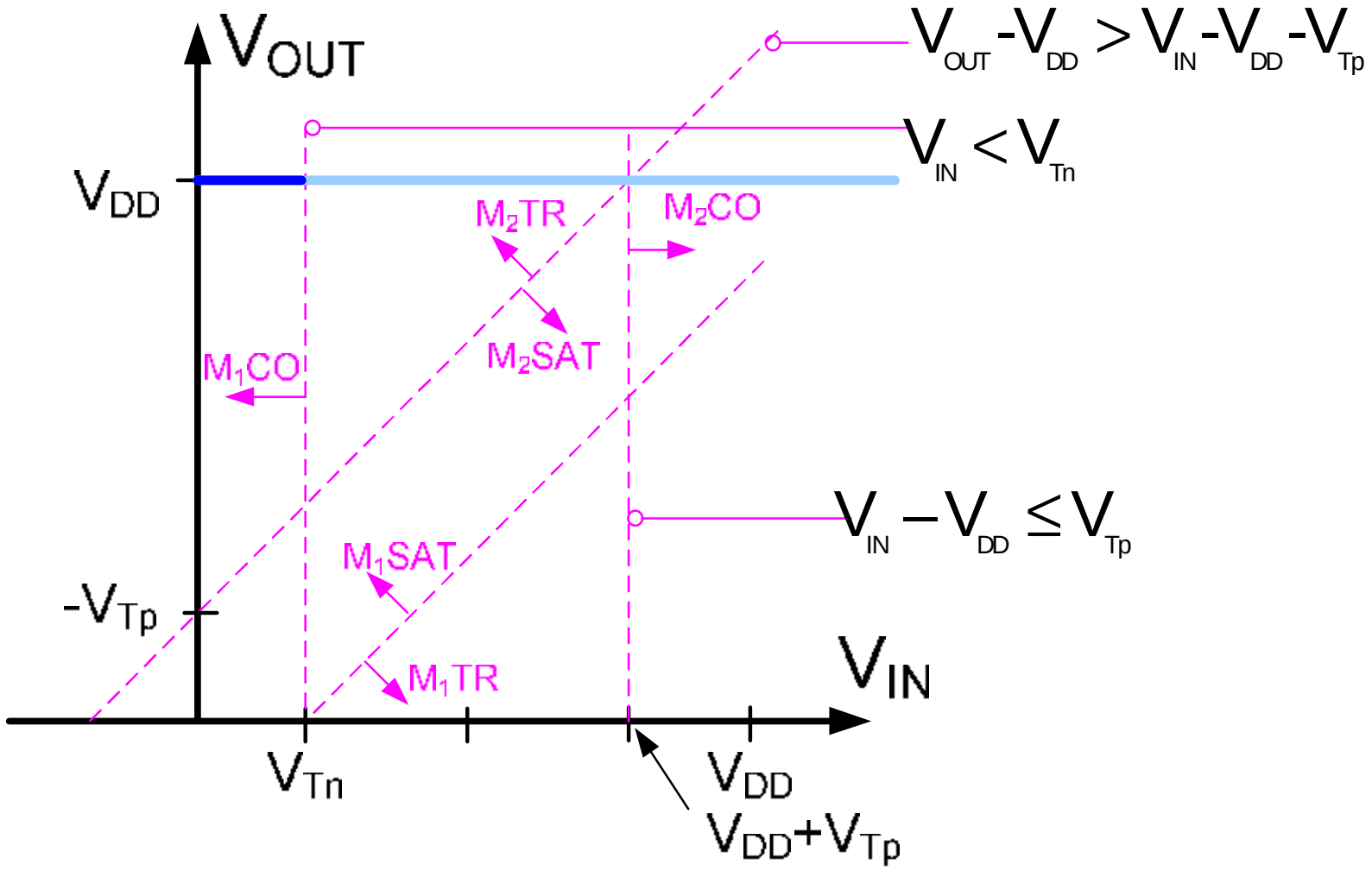
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

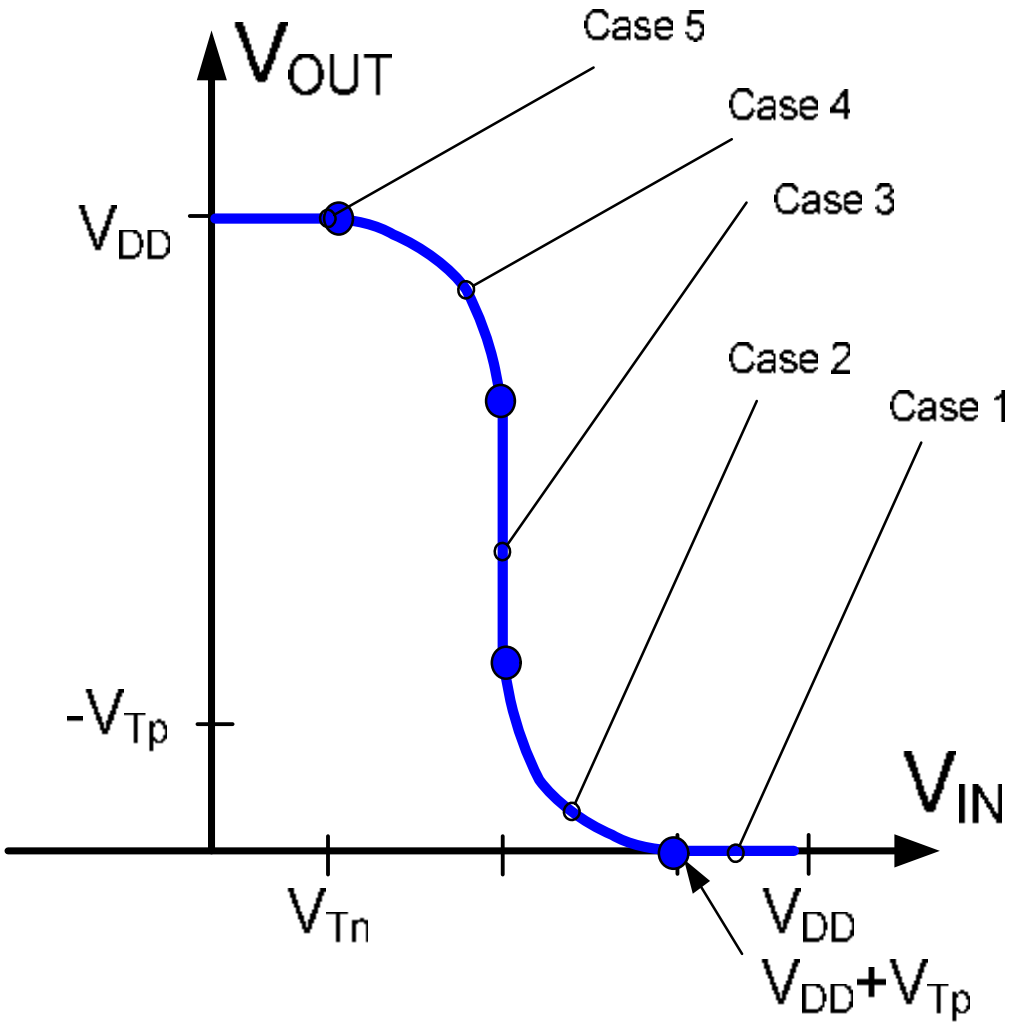
(Neglect effects)

Case 5 M_1 cutoff, M_2 triode



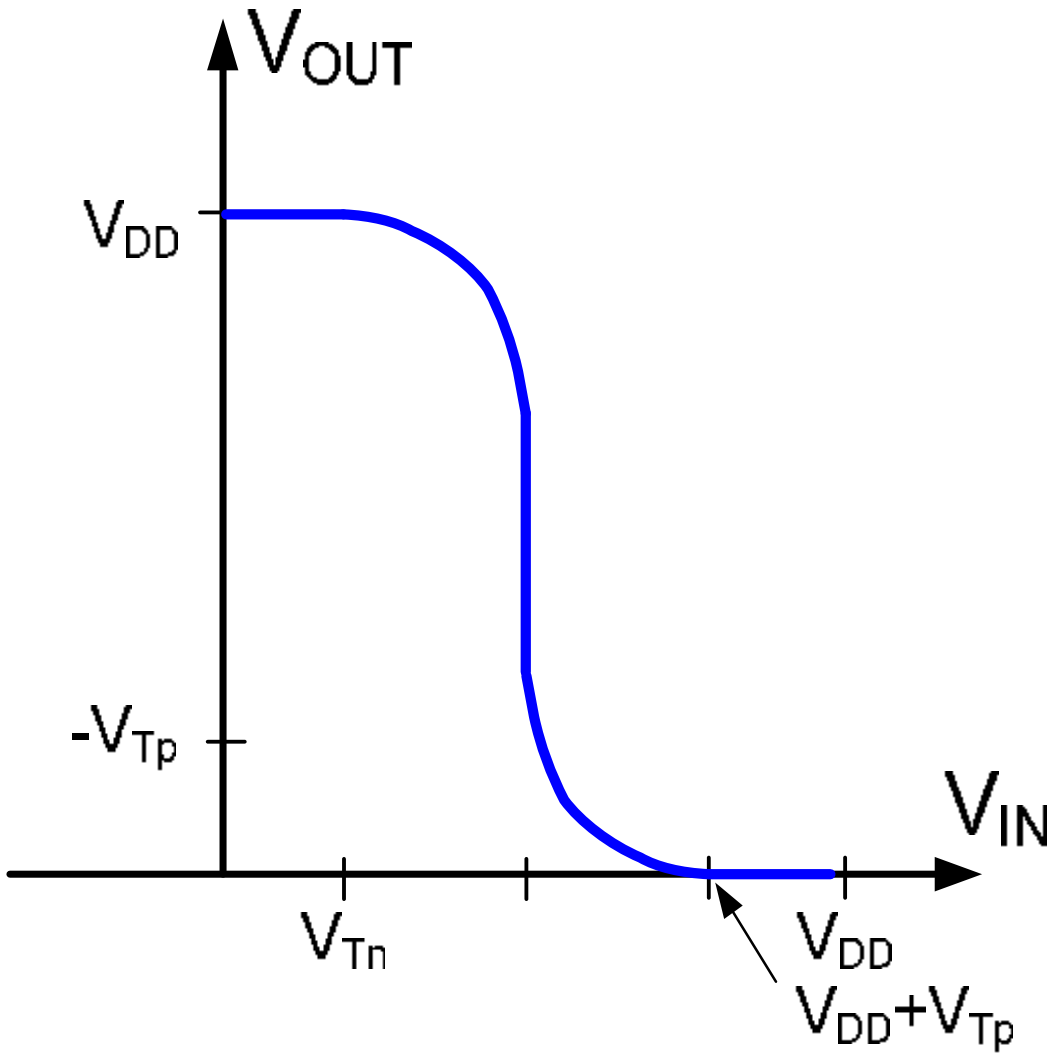
Transfer characteristics of the static CMOS inverter

(Neglect effects)



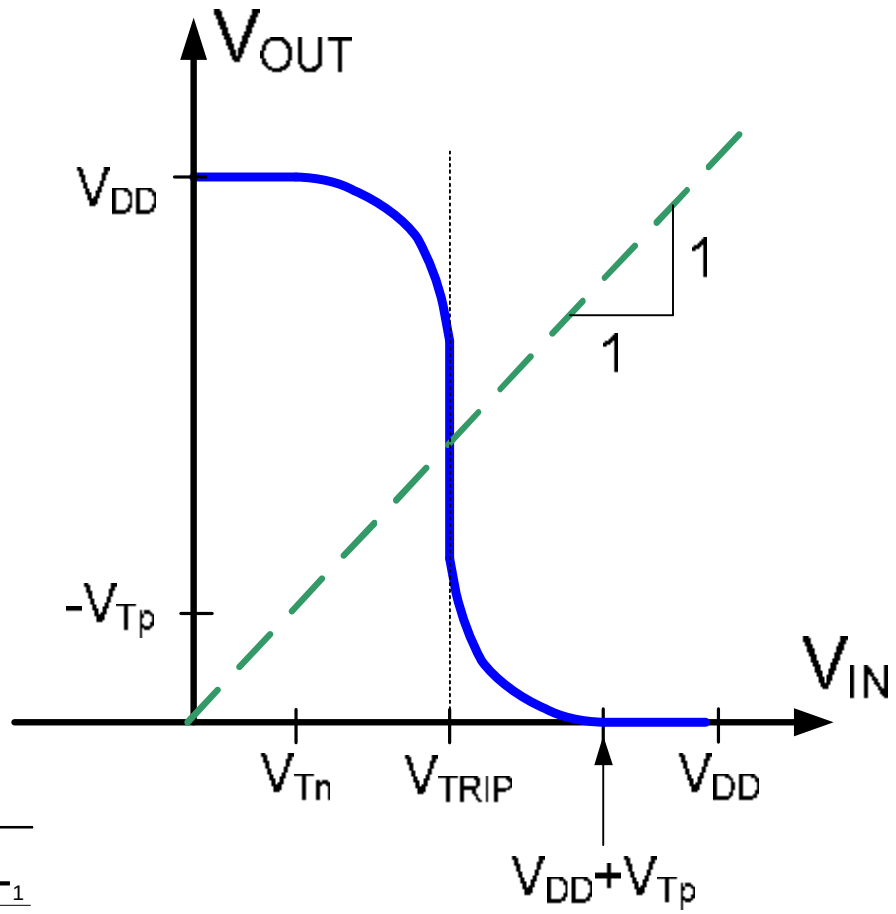
Transfer characteristics of the static CMOS inverter

(Neglect effects)



Transfer characteristics of the static CMOS inverter

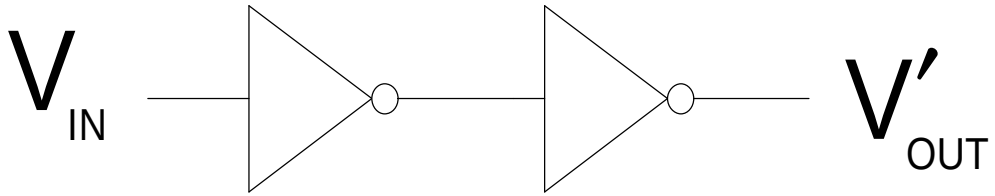
(Neglect effects)

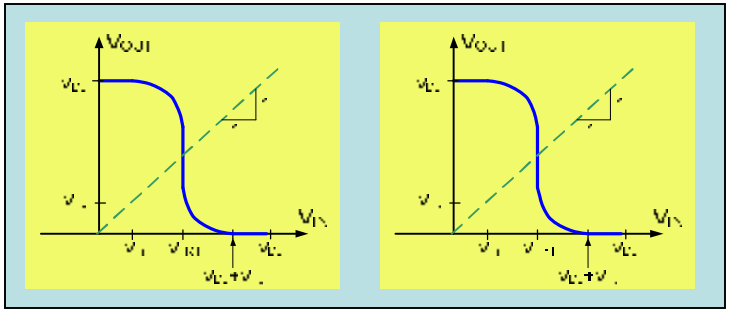


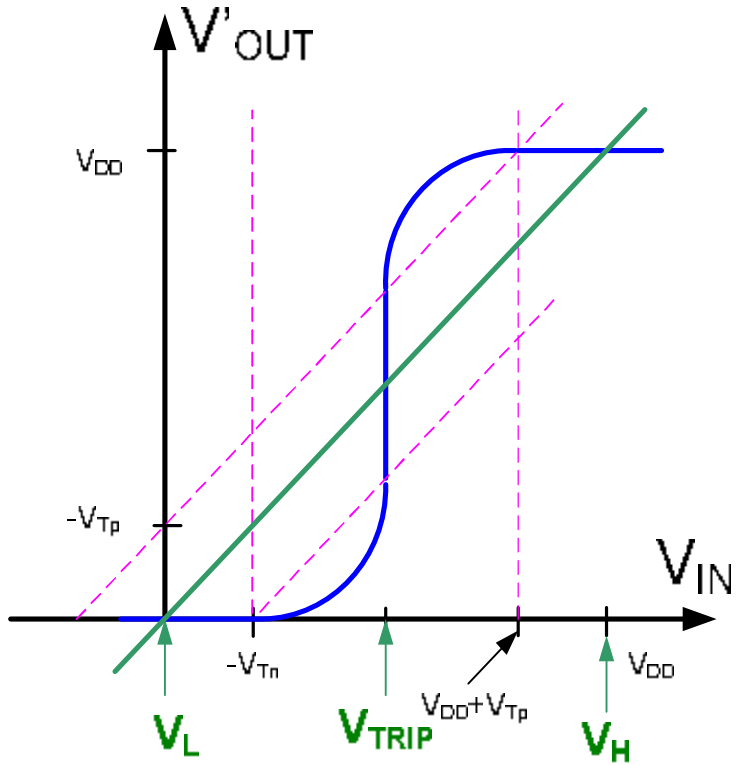
From Case 3 analysis:

$$V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

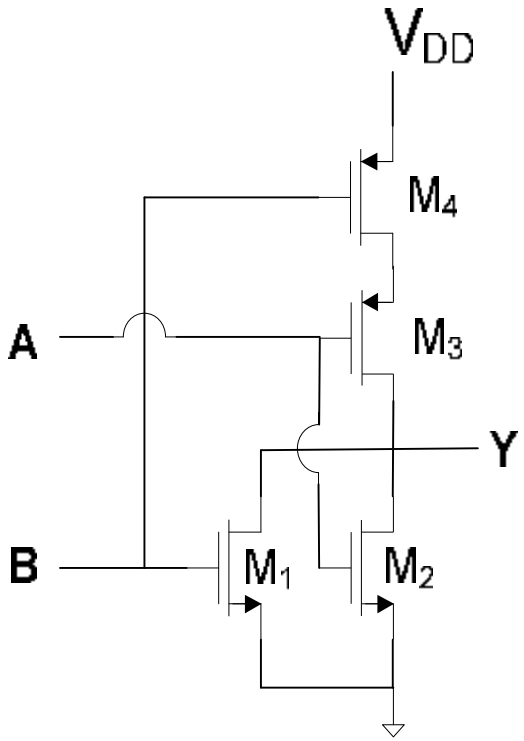
Inverter Transfer Characteristics of Inverter Pair





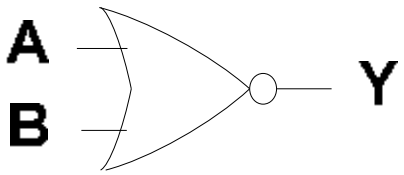


Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

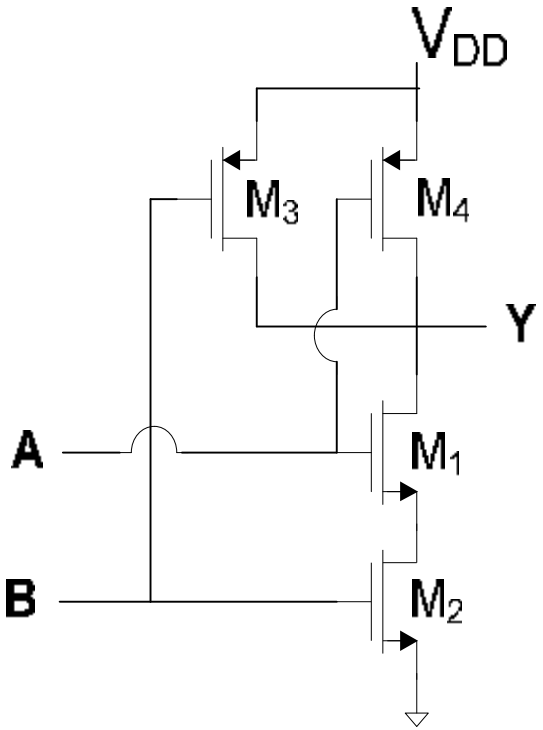
Truth Table



Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate

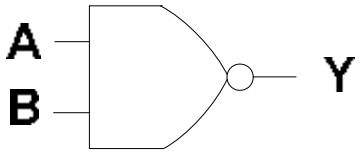
Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

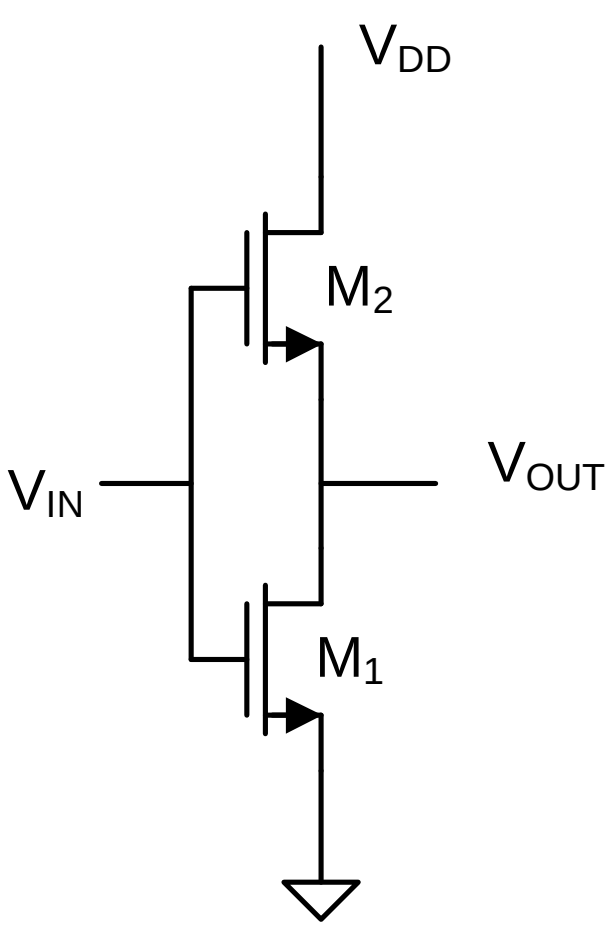
Truth Table

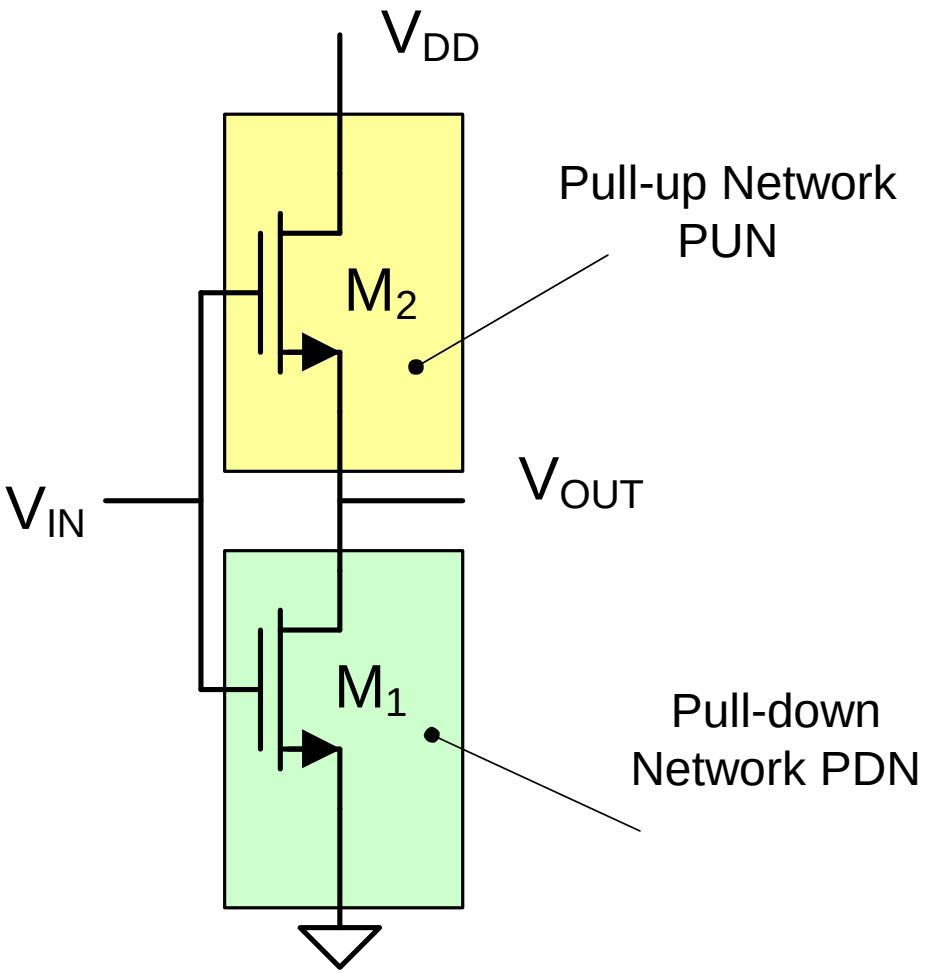
Performs as a 2-input NAND Gate



Can be easily extended to an n-input NAND Gate

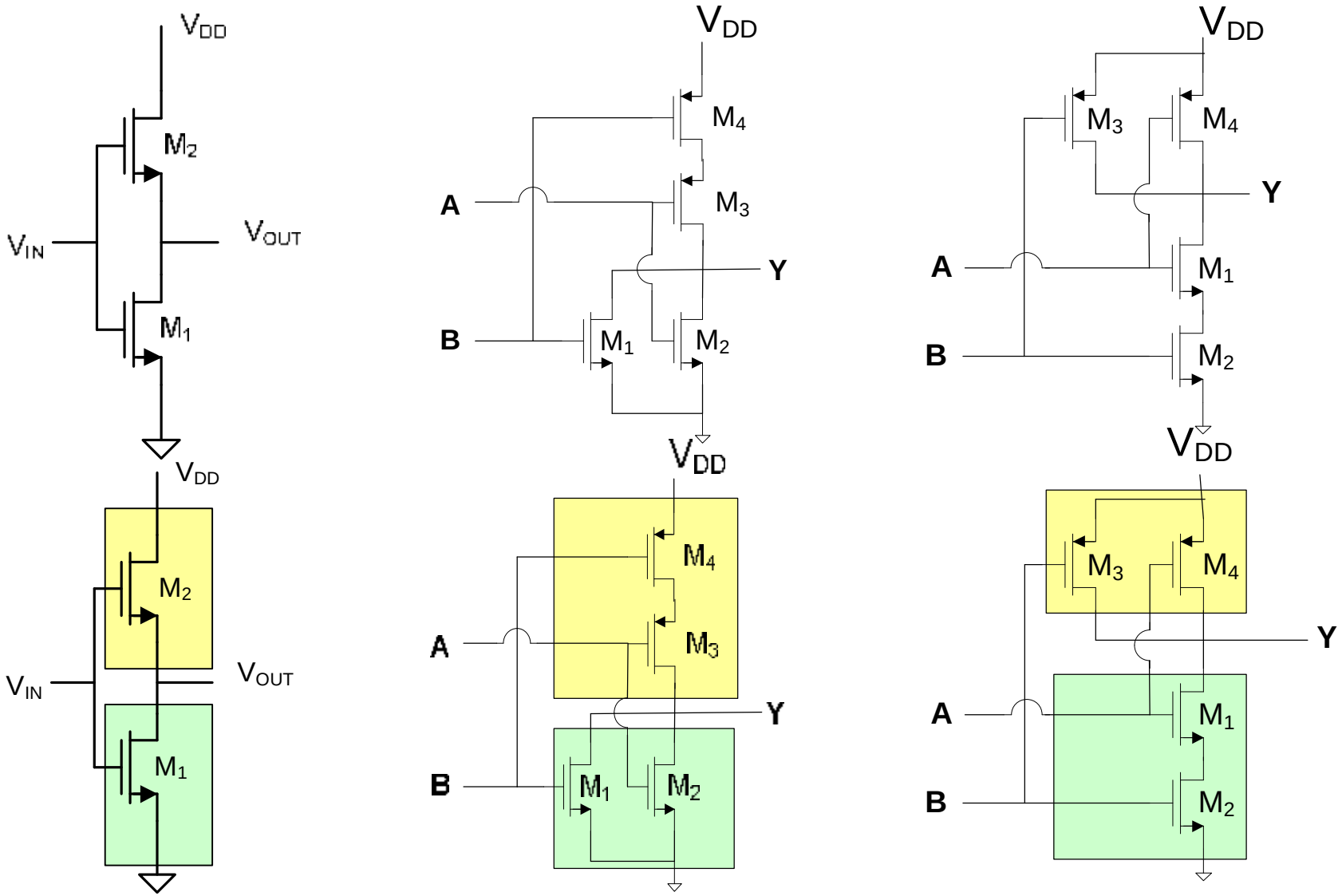
Static CMOS Logic Family





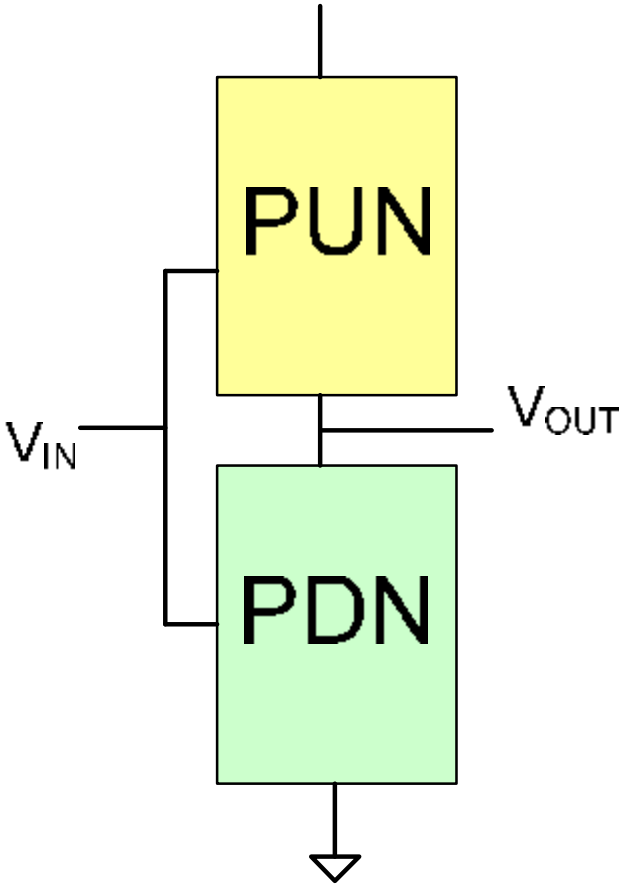
Observe PUN is p-channel, PDN is n-channel

Static CMOS Logic Family

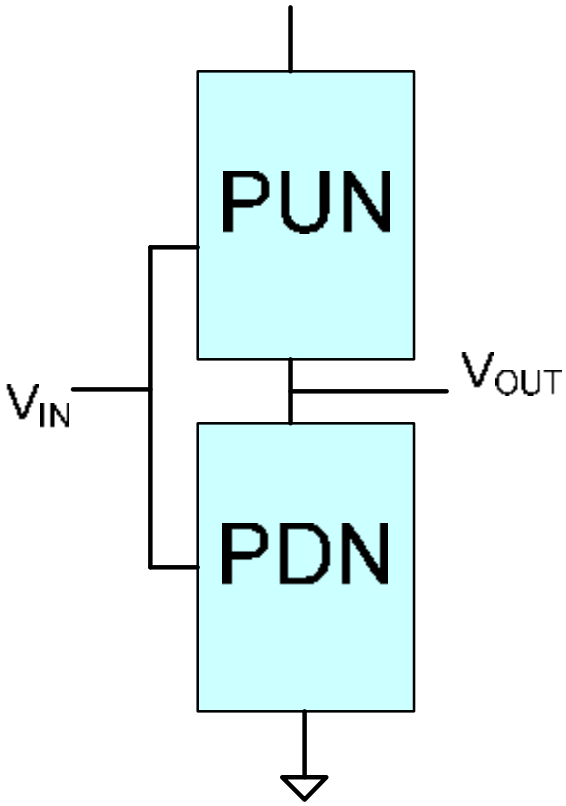


n-channel PDN and p-channel PUN

General Logic Family

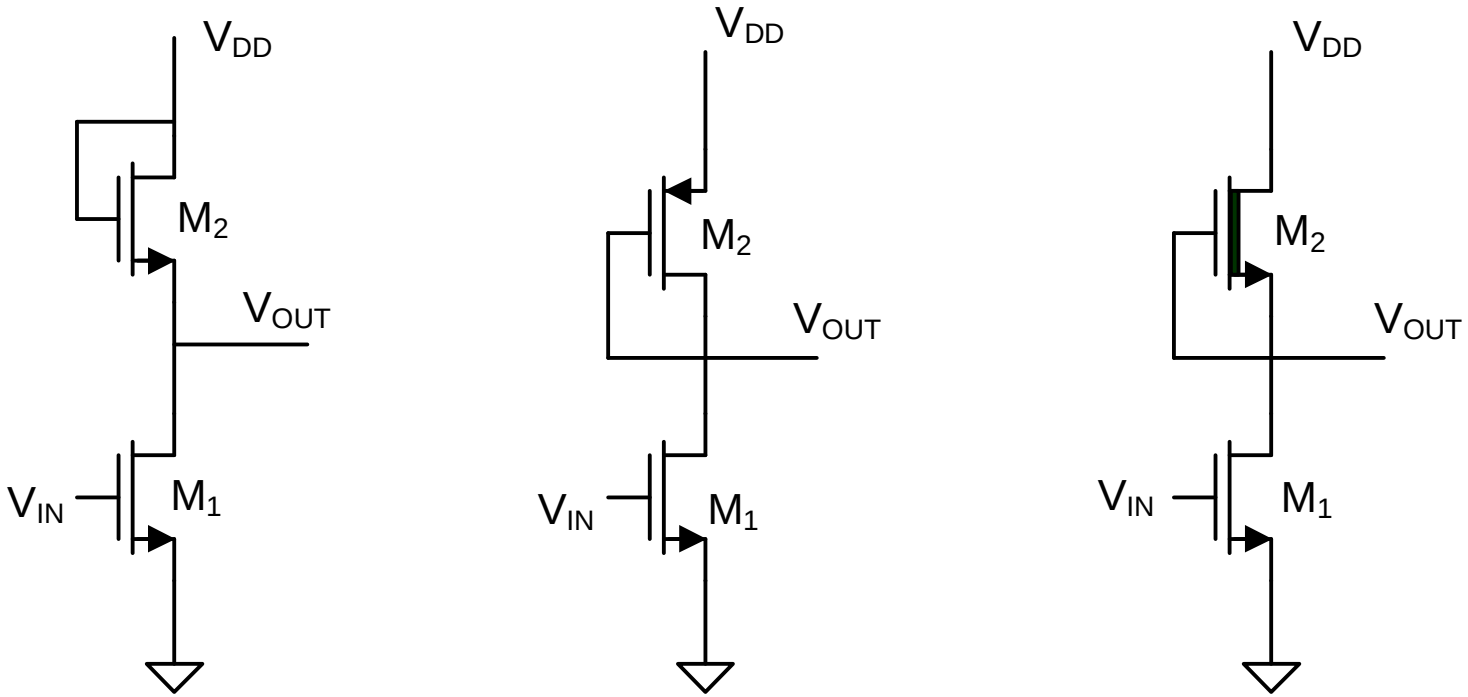


p-channel PUN
n-channel PDN

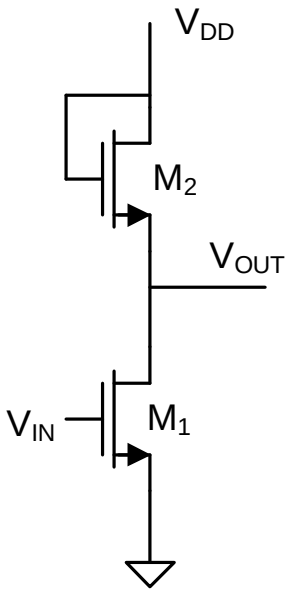


Arbitrary PUN
and PDN

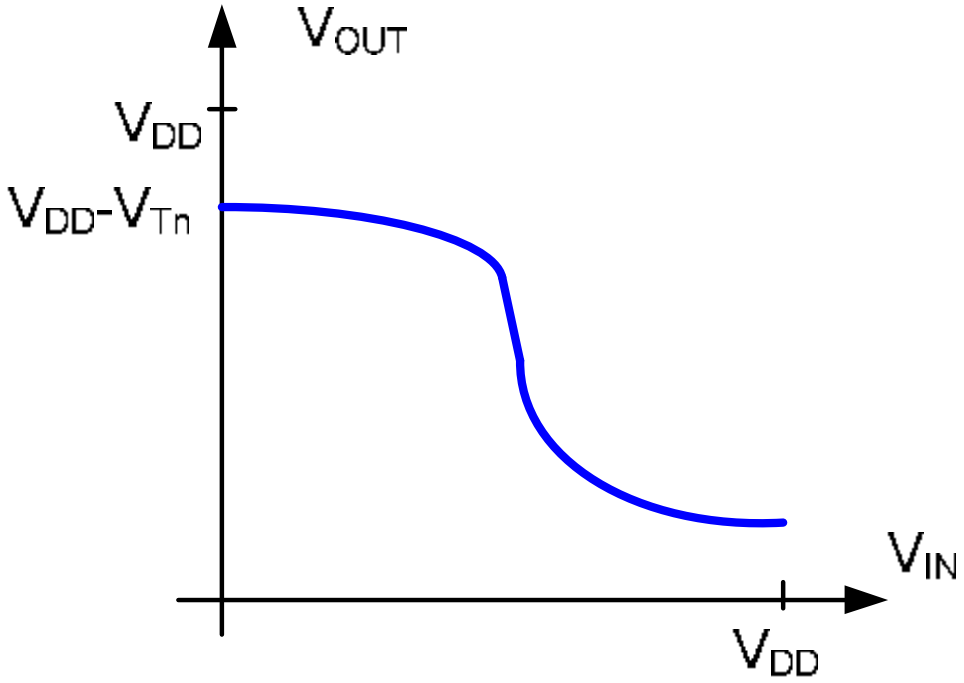
Other CMOS Logic Families



Other CMOS Logic Families

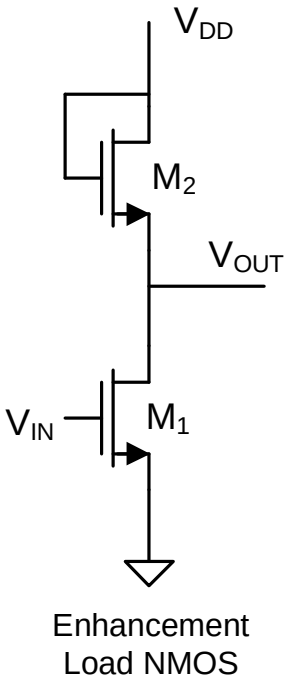


Enhancement
Load NMOS

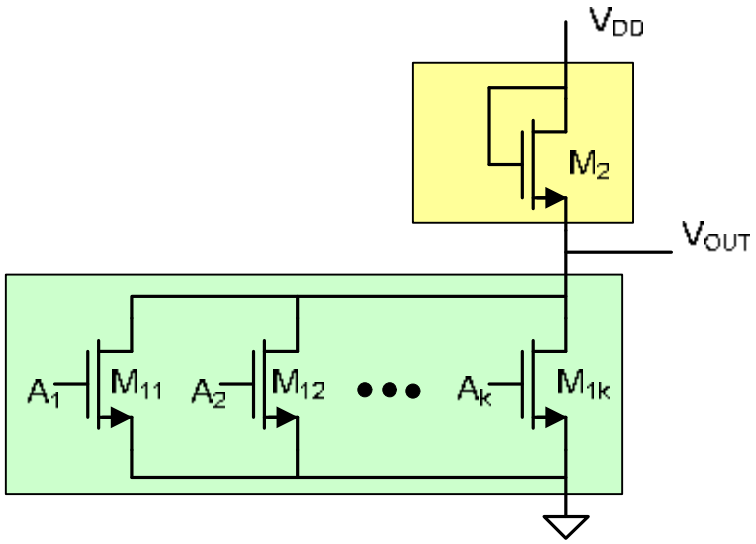


- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when V_{OUT} is low
- Very economical process
- Termed “ratio logic”
- Compact layout (no wells !)

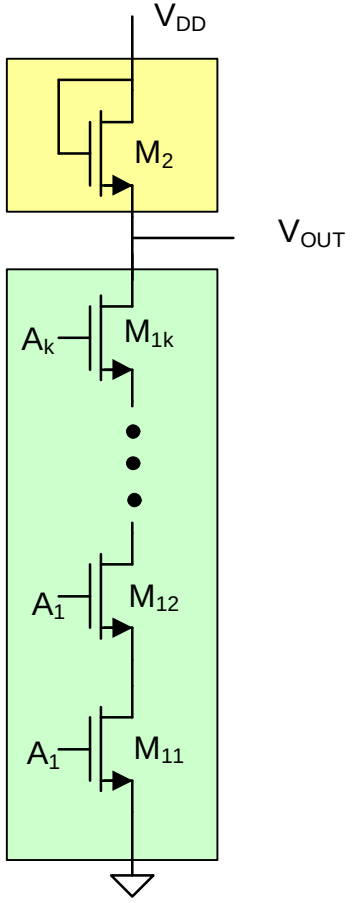
Other CMOS Logic Families



Enhancement Load NMOS



k-input NOR

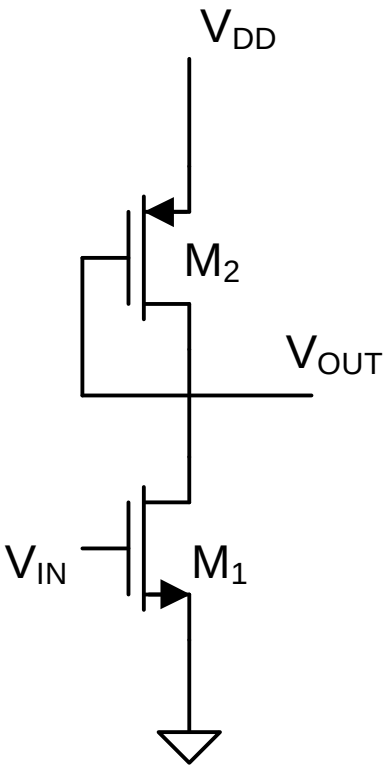


k-input NAND

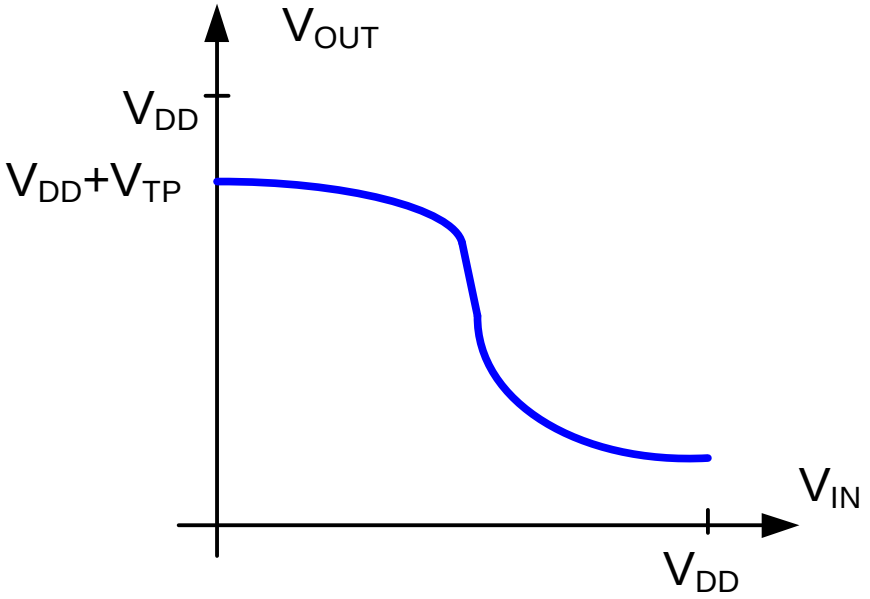
- **Multiple-input gates require single transistor for each additional input**

- **Still useful if many inputs are required (static power does not increase with k**

Other CMOS Logic Families



Enhancement Load
Pseudo-NMOS



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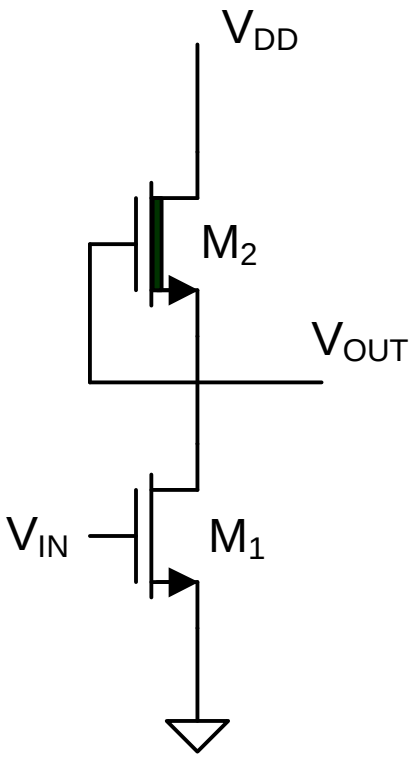
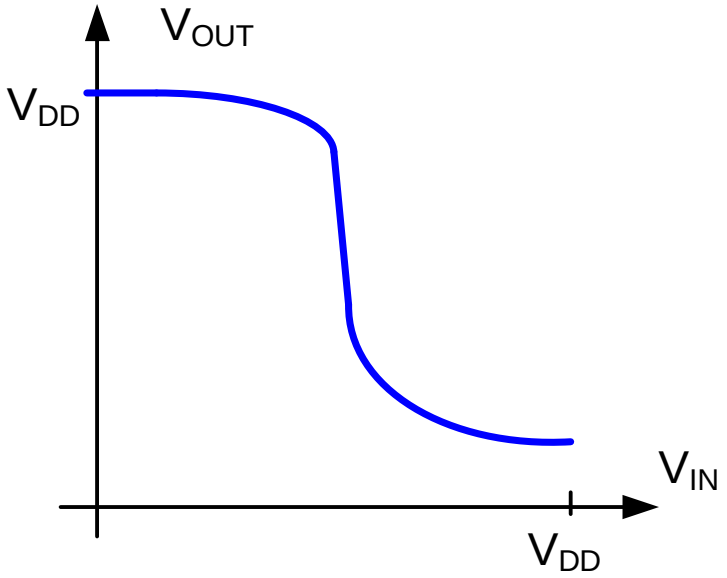
Other CMOS Logic Families



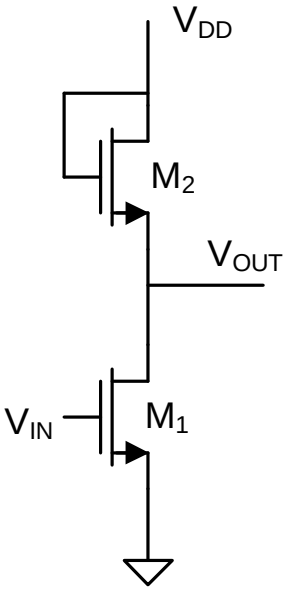
Depletion
Load NMOS



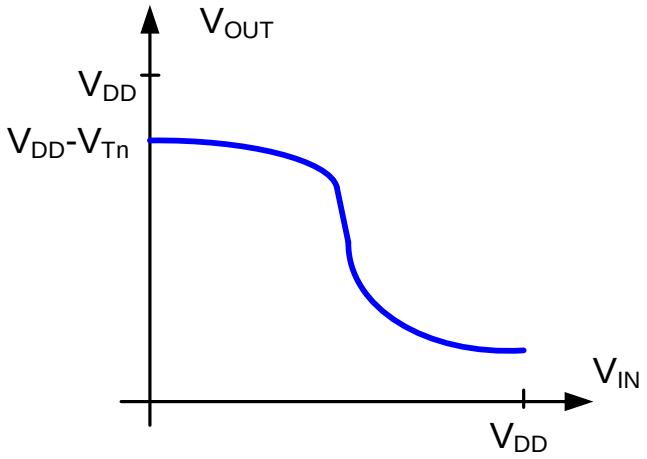
$V_{TD}<0$

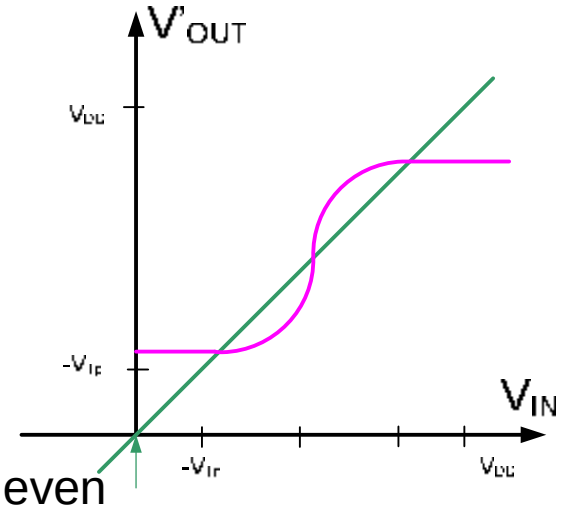
- Low swing is reduced
- Static Power Dissipation Large when V_{OUT} is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells !)
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today

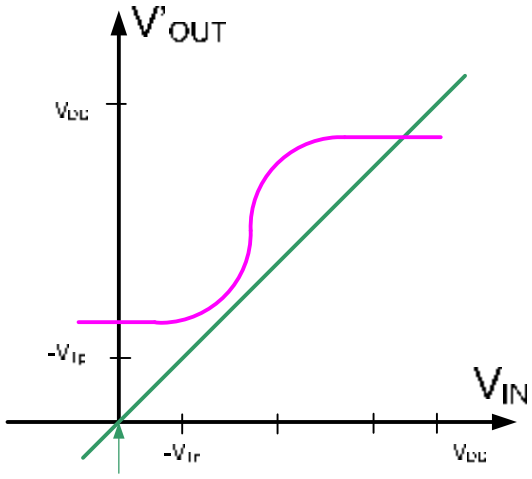
Other CMOS Logic Families



Enhancement
Load NMOS

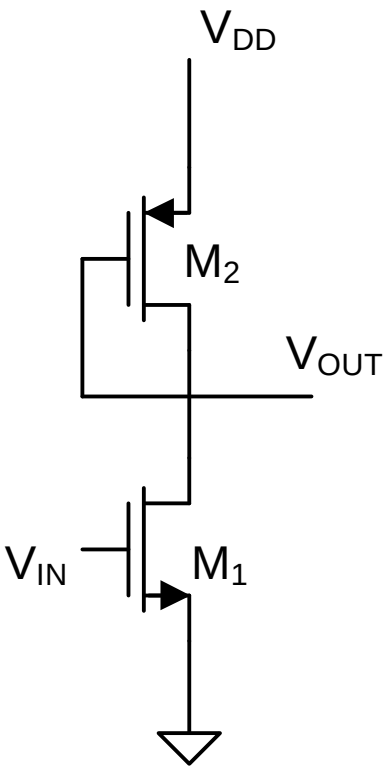




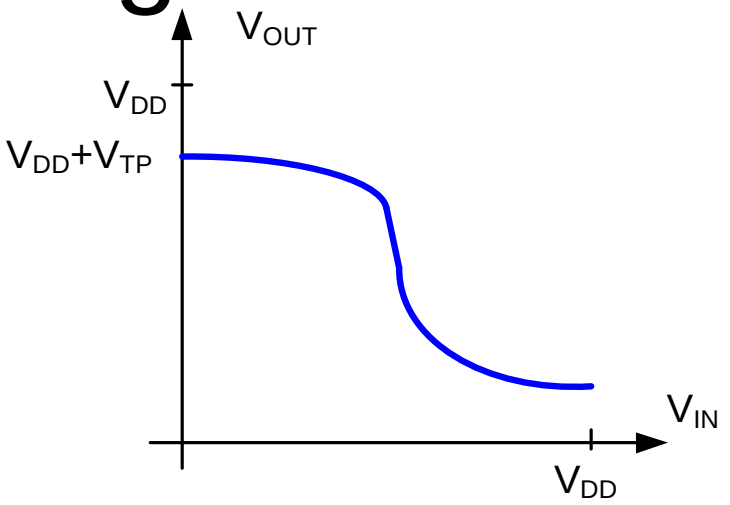


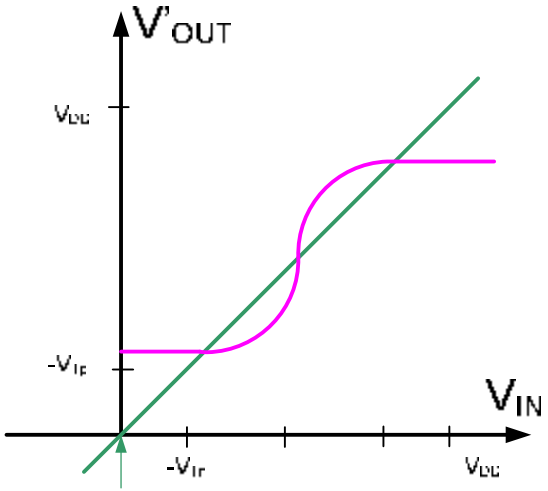
- Reduced V_H-V_L
- Device sizing critical for even basic operation
- Shallow slope at V_{TRIP}

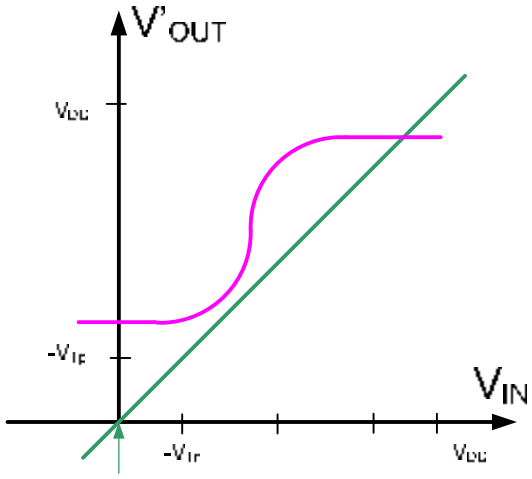
Other CMOS Logic Families



Enhancement Load
Pseudo-NMOS







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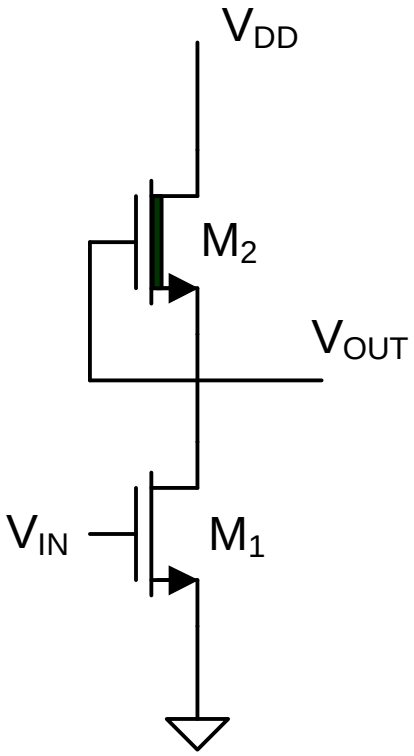

Depletion
Load NMOS

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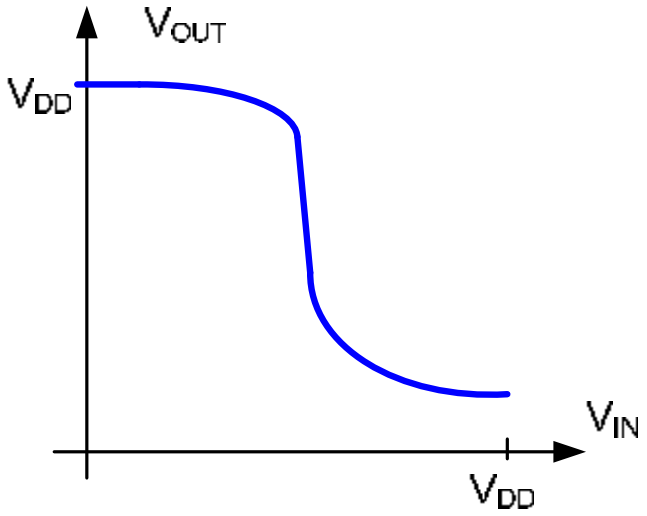

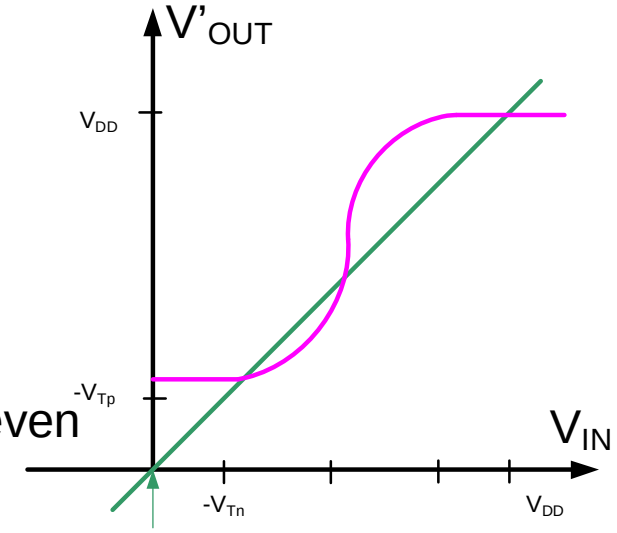

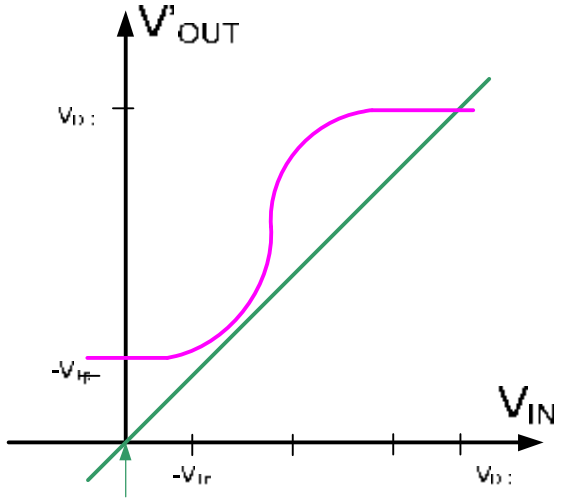

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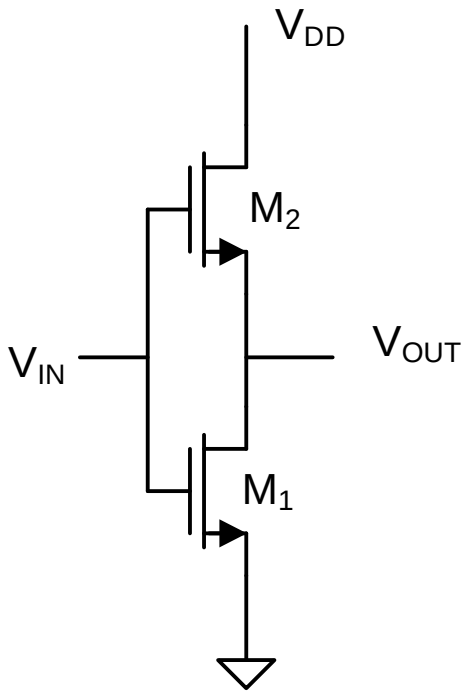
Static Power Dissipation in Static CMOS Family



When V_{OUT} is Low, $I_{D1}=0$

When V_{OUT} is High, $I_{D2}=0$

Thus, $P_{STATIC}=0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant

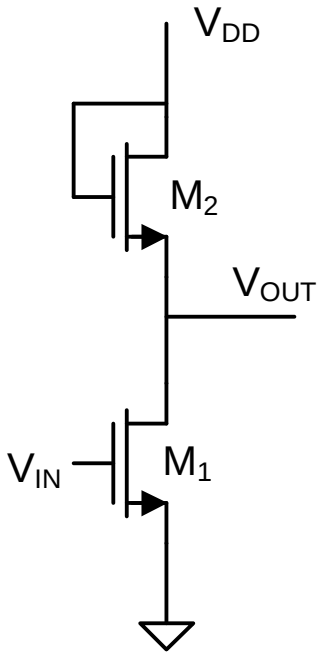
It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of n-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Static Power Dissipation in Ratio Logic Families

Example:

Assume V_{DD}=5V

V_T=1V, C_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that $V_L=V_{Tn}$



Enhancement Load NMOS

Observe:

$V_H=V_{DD}-V_{Tn}$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

$$I_{D1}=\frac{\mu C_{OX} W_1}{L_1}\left(V_{GS1}-V_T-\frac{V_{DS1}}{2}\right)V_{DS1}$$

$$I_{D1}=10^{-4}\left(5-1-1-\frac{1}{2}\right)\bullet 1=0.25mA$$

P_L=(5V)(0.25mA)=1.25mW

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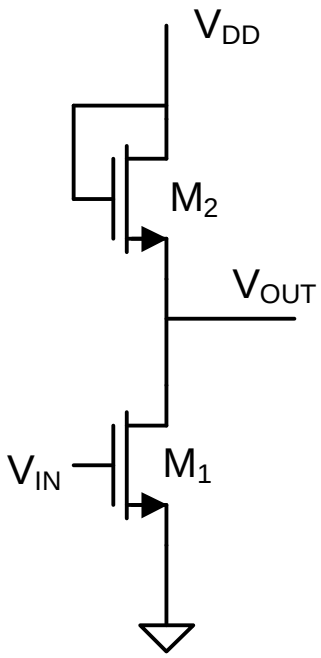

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If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

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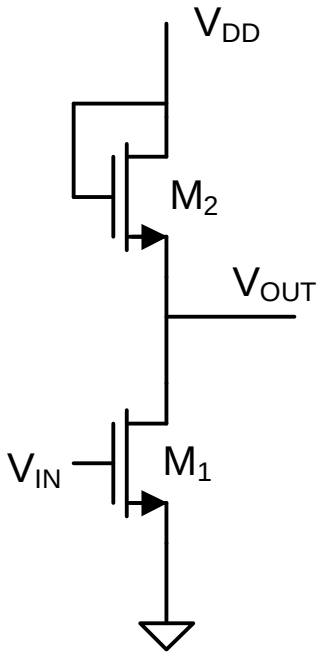


Enhancement Load NMOS

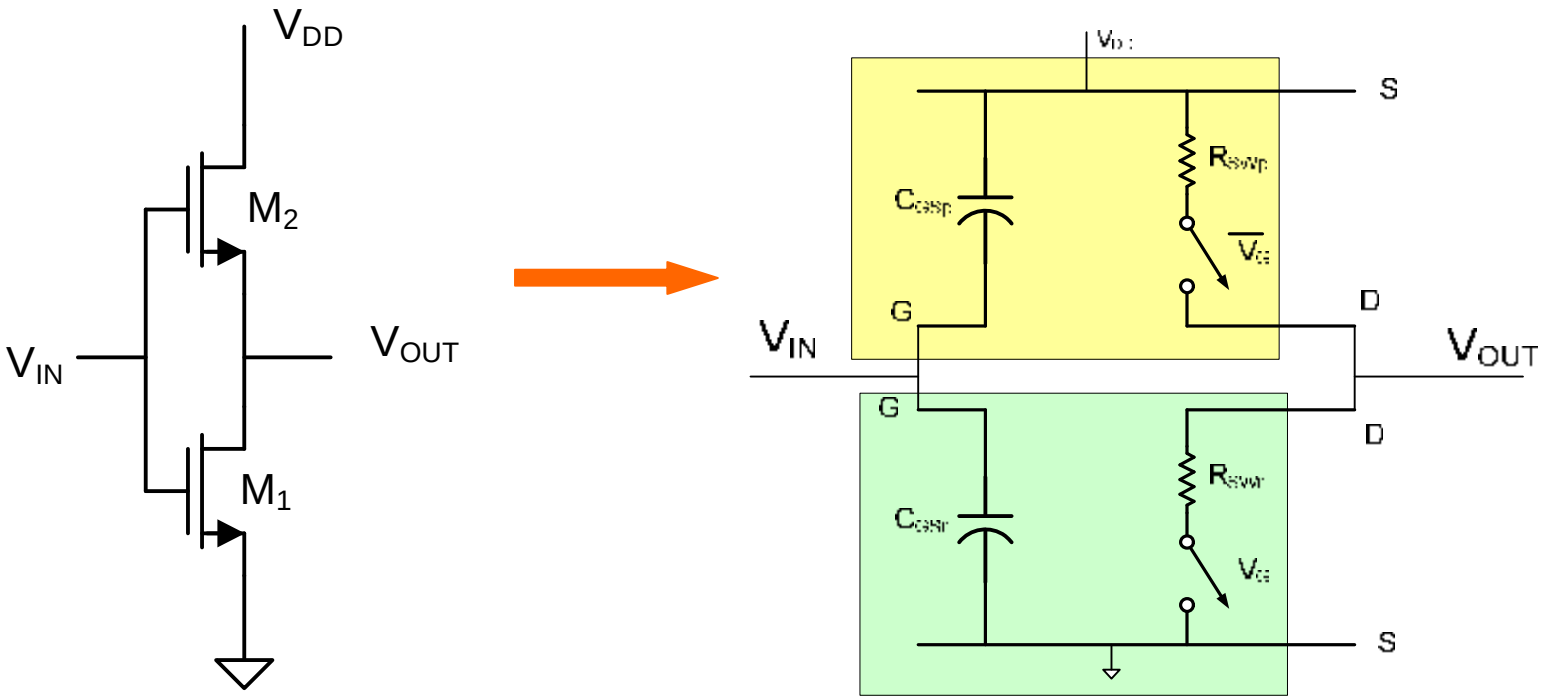
P_L=(5V)(0.25mA)=1.25mW

If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2}10^5 \bullet 1.25mW = \mathbf{62.5W}$$

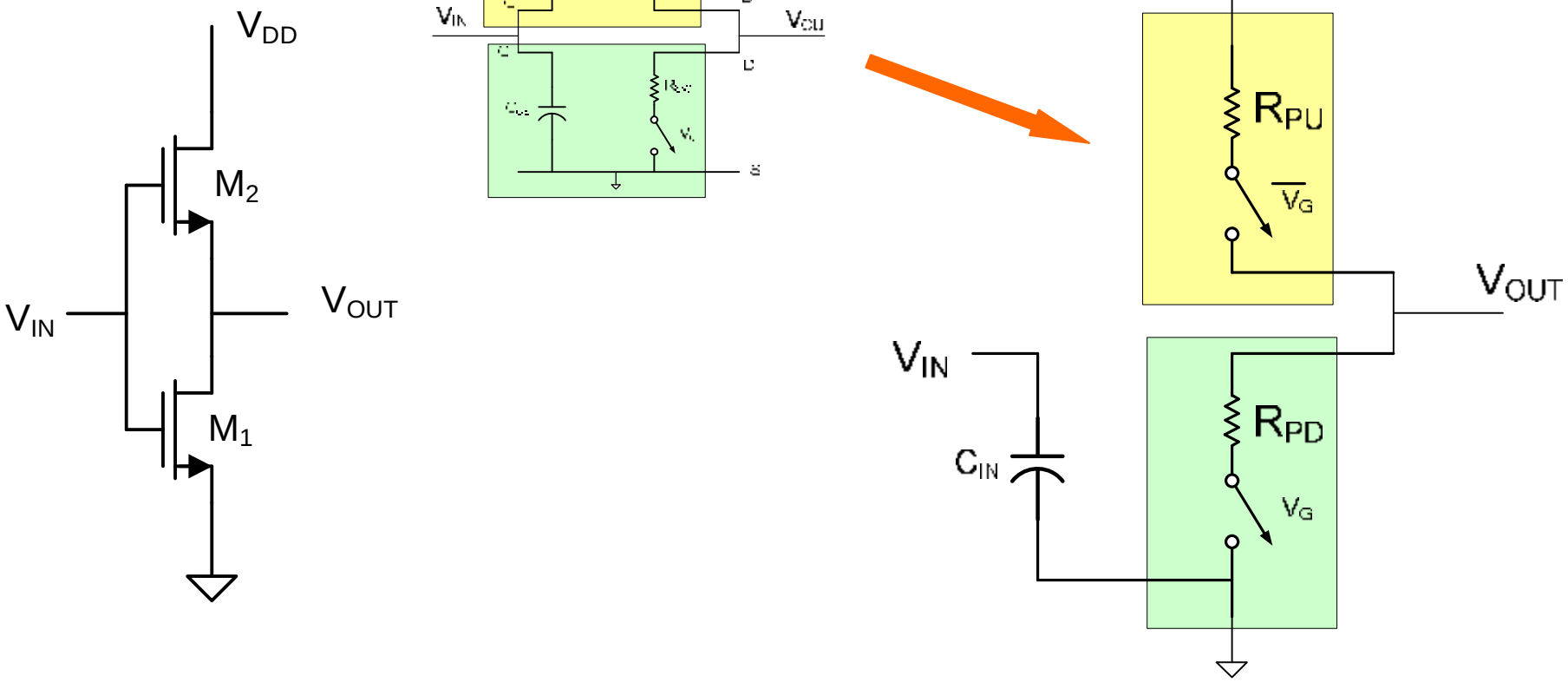
This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today

Propagation Delay in Static CMOS Family



Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family



Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)